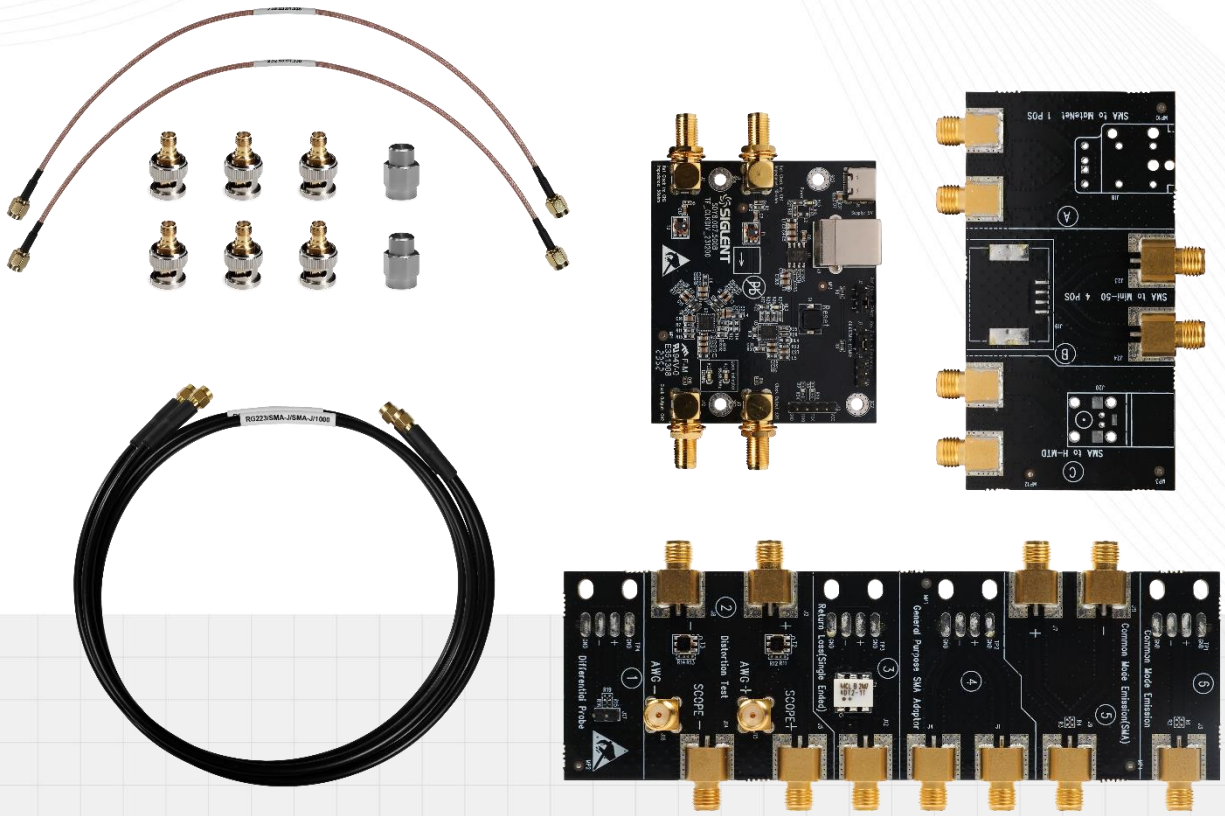
Automotive Ethernet Compliance Test Application

User Manual

EN01A



SIGLENT TECHNOLOGIES CO.,LTD

Contents

1 Introduction

Siglent provides 100BASE-T1 and 1000BASE-T1 Automotive Ethernet Compliance Test Application to verify the Automotive Ethernet transmitter device under test (DUT) compliance to specifications. The equipment required for Ethernet conformance tests including Siglent SDS7000A Oscilloscope with Ethernet Compliance Test Application software installed, FX-AMETH test fixture kit, Vector Network Analyzers, probes, SMA cables, Arbitrary Waveform Generator, Spectrum Analyzer(optional).

Siglent's Automotive Ethernet Compliance Test Solution which is compliant to 100BASE-T1 of IEEE and TC8 ECU specifications, and it's also compliant to 1000BASE-T1 of IEEE specification.

The Automotive Ethernet Compliance Test Application from Siglent:

- Let's you select individual or multiple tests to run.
- Shows you how to connect the Oscilloscope to the device under test (DUT).
- Automatically sets up the Oscilloscope for every test project.
- Provides detailed information for every test that has been run, and lets you know the thresholds at which marginal or critical warnings appear.
- Creates HTML or XML test reports of the tests that have been run.

The reference standards for Automotive Ethernet Compliance Test in this document are as follows:

- 100BASE-T1：IEEE 802.3bw, and TC8(OPEN Alliance, Automotive Ethernet ECU Test Specification, v3.0).
- 1000BASE-T1：IEEE 802.3bp.

2 Test Items and Standards Reference

2.1 100BASE-T1

2.1.1 Test Items

Siglent's 100BASE-T1 Compliance Test Solution which is compliant to IEEE802.3bw specification, and it's also in accordance to the test items of OPEN Alliance's TC8 ECU specification. The compliance test software cooperates with the FX-AMETH test fixture kit, supports the following test items:

- Test mode 1: Transmitter output positive/ negative droop tests.
- Test mode 2: Transmit clock frequency and transmitter timing jitter tests (Master mode).
- TX_TCLK jitter and TX_TCLK frequency tests (Slave mode).
- Test mode 4: Transmitter distortion test.
- Test mode 5: Transmitter power spectral density test, transmitter peak differential output test, MDI common mode emission test.
- Slave mode: MDI return loss test, MDI mode conversion loss.

2.1.2 Standards Reference

Siglent's 100BASE-T1 Automotive Ethernet Compliance Test Solution follows the IEEE802.3bw specification and the TC8 "OPEN Alliance Automotive Ethernet ECU Test Specification".
The reference standards for every test item are shown in Table 2-1.

Table 2-1 Standards reference for 100BASE-T1 Compliance Test

Reference Standard		Test Mode	Description
IEEE Std 802.3bw	OPEN Alliance TC8		
Section 96.5.4.1	OABR_PMA_TX_01	1	Transmitter output positive/negative droop tests
Section 96.5.4.3	OABR_PMA_TX_02	2	Transmitter timing jitter (Master) test
Section 96.5.4.5	OABR_PMA_TX_03	2	Transmit clock frequency (Master) test
Section 96.5.4.3		Slave	TX_TCLK timing jitter (Slave) test
Section 96.5.4.5		Slave	TX_TCLK frequency (Slave) Test
Section 96.5.4.2	OABR_PMA_TX_08	4	Transmitter distortion test
Section 96.5.4.4	OABR_PMA_TX_04	5	Transmitter power spectral density (PSD) test
Section 96.5.6		5	Transmitter peak differential output voltage test
Section 96.8.2.1	OABR_PMA_TX_05	Slave	MDI return loss test
Section 96.8.2.2	OABR_PMA_TX_06	Slave	MDI mode conversion loss test
	OABR_PMA_TX_07	5	MDI common mode emission test

2.2 1000BASE-T1

2.2.1 Test Items

Siglent's 1000BASE-T1 Compliance Test Solution which is compliant to IEEE802.3bp specification. The compliance test software cooperates with the FX-AMETH test fixture kit, supports the following test items:

- Test mode 1: TX_TCLK125 frequency and transmit timing jitter tests (Master and Slave mode).
- Test mode 2: Transmit clock frequency test, transmitter MDI output jitter test.
- Test mode 4: Transmitter distortion test.
- Test mode 5: transmitter power spectral density test, transmitter peak differential output test.
- Test mode 6: transmitter output positive/ negative droop tests.
- Salve mode: MDI return loss test, MDI mode conversion loss test.

2.2.2 Standard Reference

Siglent's 1000BASE-T1 Automotive Ethernet Compliance Test Solution follows the IEEE802.3bp specification.

The reference standard for every test item is shown in Table 2-2.

Table 2-2 Standard Reference for 1000BASE-T1 Compliance Test

Reference Standard	Test Mode	Description
IEEE Std 802.3bp, Section 97.5.3.6	1	TX_TCLK125 frequency test
IEEE Std 802.3bp, Section 96.5.3.3	1	Transmitter timing jitter (Master) test
IEEE Std 802.3bp, Section 96.5.3.3	1	Transmitter timing jitter (Slave) test
IEEE Std 802.3bp, Section 97.5.3.6	2	Transmit clock frequency test
IEEE Std 802.3bp, Section 97.5.3.3	2	Transmitter MDI output jitter test
IEEE Std 802.3bp, Section 97.5.3.2	4	Transmitter distortion test
IEEE Std 802.3bp, Section 97.5.3.4	5	Transmitter power spectral density (PSD) test
IEEE Std 802.3bp, Section 97.5.3.5	5	Transmitter peak differential output test
IEEE Std 802.3bp, Section 97.5.3.1	6	Transmitter output positive/ negative droop tests
IEEE Std 802.3bp, Section 97.7.2.1	Slave	MDI return loss test
IEEE Std 802.3bp, Section 97.7.2.2	Slave	MDI mode conversion loss test

3 Test Equipment

3.1 Required Equipment

The 100BASE-T1 and 1000BASE-T1 Automotive Ethernet Electrical Compliance Test Solution require the following equipment:

- Oscilloscope (SDS7000A): Oscilloscope's bandwidth larger than 2GHz, and with the Ethernet Compliance Test Application software that has installed the option key (SDS7000A-CT-100BASE-T1 option for 100BASE-T1 and SDS7000A-CT-1000BASE-T1 for 1000BASE-T1).
- FX-AMETH kit: FX-AMETH kit is the Automotive Ethernet Electrical Compliance Test Fixture kit from Siglent that provides the physical connection and test points after the DUT enters the test modes.
- Differential probe or SMA cables:
  - Differential probe (e.g., SAP2500D or SAP5000D): bandwidth greater than 2 GHz for probing signals;
  - SMA cables: connects from the Oscilloscope to the test fixture for probing signals.
- Vector Network Analyzer: VNA is used for MDI return loss test, MDI mode conversion loss test.
- Spectrum Analyzer(optional): The Spectrum Analyzer can be used for transmitter power spectral density (PSD) test and MDI common mode emission test.
- Arbitrary Waveform Generator: When the transmitter distortion test requires disturbing signals, the Arbitrary Waveform Generator can be used to output two sine wave signals with 180-degree phase shift for the transmitter distortion test.
- USB Connection Cable: The cable is used to connect the USB Host port on the Oscilloscope to the USB Device port on the Vector Network Analyzer or Spectrum Analyzer, so that the Oscilloscope can control and configure the Slave Device and obtain the test data.

3.2 Delivery Checklist

The FX-AMETH kit includes the items listed in Table 3-1. When you receive the FX-AMETH kit, firstly, verify that all items listed on the checklist have been received. If you notice any omissions or damage, please contact to your nearest Siglent customer service center or distributor as soon as possible. If you fail to contact us immediately in case of omissions or damage, we will not be responsible for replacement.

Table 3-1 FX-AMETH Kit Checklist

Item name	Quantities
User Manual	1
Automotive Ethernet Test Fixture	1
Frequency Converter Test Fixture	1
Automotive Ethernet Adapter (MateNet to SMA, Mini-50 to SMA, H-MTD to SMA)	1
50Ω Terminator（SMA）	2
SMA cable (Length:1000mm)	7
SMA cable (Length:300mm)	2
BNC to SMA Adaptor	6
Jumper	2

3.3 Introduction to FX-AMETH Test Fixture Kit

3.3.1 Automotive Ethernet Test Fixture

Automotive Ethernet Test Fixture which supports the 100BASE-T1 and 1000BASE-T1 compliance tests. The Automotive Ethernet Test Fixture is shown in Figure 3-1.

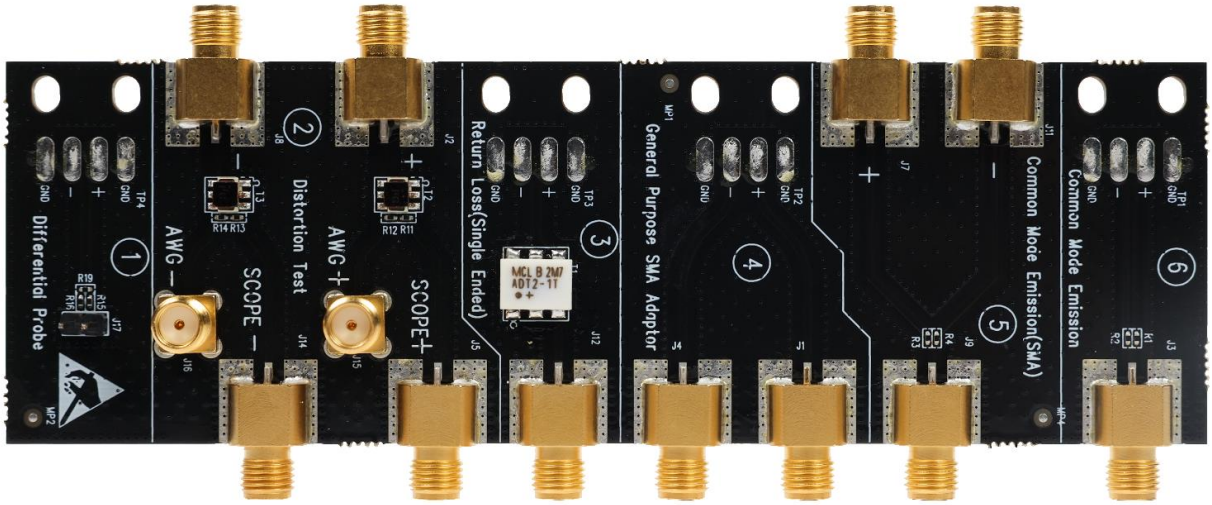


Figure 3-1 Automotive Ethernet Test Fixture

Every section on the fixture is described as follows:

Section ①: Supports soldering the Ethernet cable of the DUT directly to the Automotive Ethernet Test Fixture, an active differential probe can be used to do most of the compliance test items with this section, and a cable tie can be used to fasten the Ethernet cable to the through-hole.

Section ②: Supports the transmitter distortion test with injecting the disturbing signals to the DUT.

Section ③: Supports soldering the Ethernet cable of the DUT directly to the test fixture. This section uses a balun to perform the differential signal to single-ended signal conversion. This section can perform transmitter power spectral density (PSD) test. A cable tie can be used to fasten the Ethernet cable to the through-hole.

Section ④: Supports soldering the Ethernet cable of the DUT directly to the test fixture, using a pair of SMA cables can do most of the compliance test items with this section, and a cable tie can be used to fasten the Ethernet cable to the through-hole.

Section ⑤: Supports common mode emission test of 100BASE-T1 through SMA cables.

Section ⑥: Supports soldering the Ethernet cable of the DUT directly to the test fixture to perform the common mode emission test of 100BASE-T1. A cable tie can be used to fasten the Ethernet cable to the through-hole.

3.3.2 Frequency Converter Test Fixture

In the transmitter distortion test of 100BASE-T1 and 1000BASE-T1. In order to get higher test accuracy, it is necessary to use a Frequency Converter test fixture to convert the TX_TCLK (100BASE-T1) or TX_TCLK125(1000BASE-T1) clock of the DUT to a 10MHz clock, the 10MHz clock will be connect to the external 10MHz clock source input of the Oscilloscope and Arbitrary Waveform Generator. In this way, we get the clock domain synchronization between DUT, Oscilloscope and Arbitrary Waveform Generator.

The Frequency Converter test fixture is shown in Figure 3-2.

Figure 3-2 Frequency Converter test fixture

How to use the Frequency Converter test fixture is described as below:

(1) J6, J9: USB type-C and USB type-B connectors. It is used to input DC5V power supply to the Frequency Converter test fixture. Once the power supply is correctly connected, the LED HL3 and HL5 will light up.

(2) Connect the DUT's TX_TCLK (100BASE-T1) or TX_TCLK125(1000BASE-T1) to the input

channel of J1(CH1) or J2(CH2) on the Frequency Converter. When the jumper is installed on J5(pin1,2), the CH2 with 50ohm input impedance will be selected. When the jumper is installed on J5(pin2,3), the CH1 with 10kohm input impedance will be selected.

(3) J1(CH1 Reference Clock input): SMA connector, the input impedance of this channel is 10kΩ, install the jumper at J5(pin 2, 3) to select CH1, the amplitude of input signal is 0.2Vp-p~3.3Vp-p.

(4) J2(CH2 Reference Clock input): SMA connector, the input impedance of this channel is 50Ω, install the jumper at J5(pin 1,2) to select CH2, the amplitude of input signal is 0.4Vp-p~3.3Vp-p.

(5) J7: Input reference clock frequency selection:

- When the jumper is installed at J7(pin 1, 2), the input clock frequency of CH1 or CH2 is 66.667MHz.
- When the jumper is installed at J7(pin 2, 3), the input clock frequency of CH1 or CH2 is 125MHz.

(6) J3(10Mz Clock Output: CH1): The output impedance is 50Ω, the output square voltage level is 0V and 3.3V(without 50Ωtermination).

(7) J12(10Mz Clock Output: CH2): The output impedance is 50Ω, the output square voltage level is 0V and 3.3V(without 50Ωtermination).

(8) The LEDs indication are as follows:

- HL5: Input 5V power supply indication.
- HL3: The 5V to 3.3V transition indication
- HL1: When the LED HL1 lights up, which indicates the frequency conversion from 66.667MHz to 10MHz to the output channels work well.
- HL2: When the LED HL2 lights up, which indicates the frequency conversion from 125MHz to 10MHz to the output channels work well.

(9) S1: Reset Switch that allows to reset and re-configure PLL chip on the board to work properly.

The specification of Frequency Converter test fixture is as Table 3-2.

Table 3-2 Specification of Frequency Converter test fixture

Input Power characteristic	Specification
Input voltage	5V
Current consumption(max)	100mA
Connector	Type-B and Type-C receptacle
Clock input Characteristic	Specification
Number of input clock channels (Through install jumper on J5 to select)	2
Input connector	SMA
Input impedance (Through install jumper on J5 to select)	CH1:10kΩ CH2:50Ω
Input coupling	AC

Input voltage range	CH1: 0.2V~3.3V CH2:0.4V~3.3V
Supported input clock frequencies (Through install jumper on J7 to select)	66.667MHz or 125MHz
Input duty cycle	40%~60%
Clock output Characteristic	Specification
Number of output clock channels	2
Out connector	SMA
Output impedance (LVCMOS)	45Ω (min), 50Ω (typ), 75Ω (max)
Output voltage range	3.3V(unterminated) 1.65V(50Ω terminated)
Output clock frequency	10MHz
Output clock rise time (50Ω terminated)	<1ns

3.3.3 Automotive Ethernet Adapter

In order to facilitate the use of connectors with different standard interfaces such as MateNet (TE), Mini-50(Molex), H-MTD(Rosenberger) to do the automotive Ethernet compliance test, Siglent also provides an Automotive Ethernet Adapter to make connection between the transmitter under test (DUT) and the Oscilloscope. The SMA connectors has been soldered on the Automotive Ethernet Adapter. User can solder three kinds of the connectors according to the test requirements. The Adapter cooperates with the Automotive Ethernet Test Fixture and Frequency Converter test fixture for Automotive Ethernet Compliance test on SDS7000A Oscilloscope.

For the other different kinds of the available adapters, you can also use any similarly customized adapter to do the test.

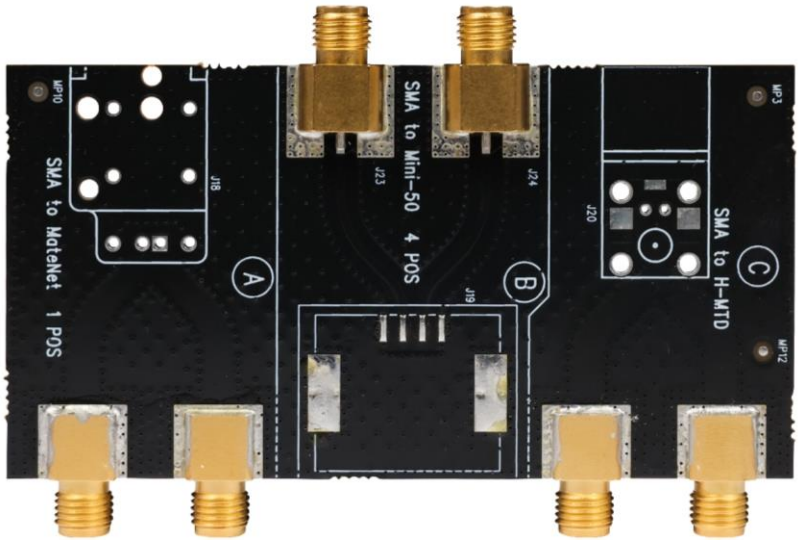


Figure 3-3 Automotive Ethernet Adapter

4 Compliance Test Software

Siglent's Automotive Ethernet Compliance Test Application is a solution based on IEEE802.3bw, IEEE802.3bp and OPEN Alliance's TC8 specifications. The Ethernet Compliance Test Application software controls the Oscilloscope to automatically perform the tests. The graphical operation guide simplifies the measurement process, the test items can be flexibly configured, and the test report records the entire measurement results, including the test values and the screenshots of the test waveforms.

SDS7000A provides 100BASE-T1 and 1000BASE-T1 Compliance Test solution, the user can select the compliance test according to **Analysis** -> **Compliance Test** -> **Protocol Type**, select **100BASE-T1** or **1000BASE-T1** and click **ON** to activate the Compliance Test function, which is shown in Figure 4-1. The Compliance Test function is divided into three main parts: **Test Config** , **Results** , and **Report Setting** .

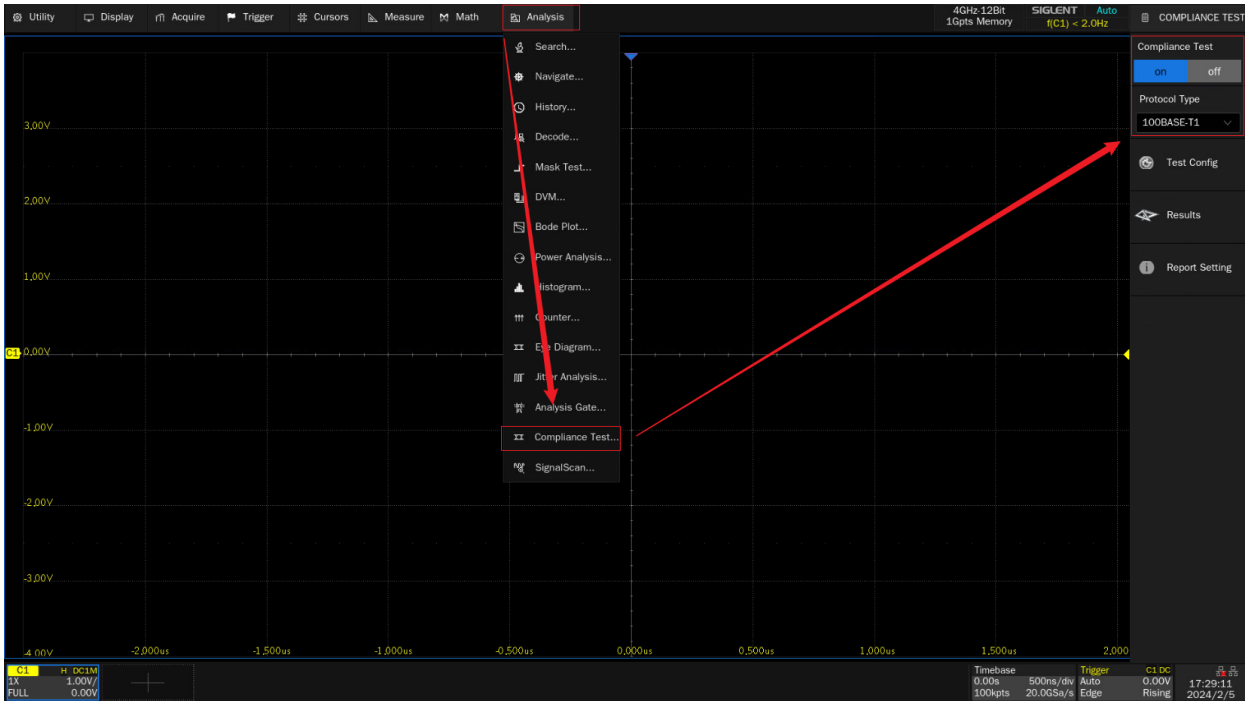


Figure 4-1 Steps for launching Compliance Analysis Software

4.1 Test Configuration

Clicking on **Test Config** will bring up the specific test configuration window, as shown in Figure 4-2, which is divided into six steps based on the test process: **Setup** , **Test Select** , **Configure** , **Connect** , **Run Test** , and **Result** .

➢ **Setup:** Provide the functions of **Recall** , **Last** and **Save** for the configuration.

For the 100BASE-T1 compliance test, Siglent also provides the selection of **IEEE** specification or

Open Alliance specification.

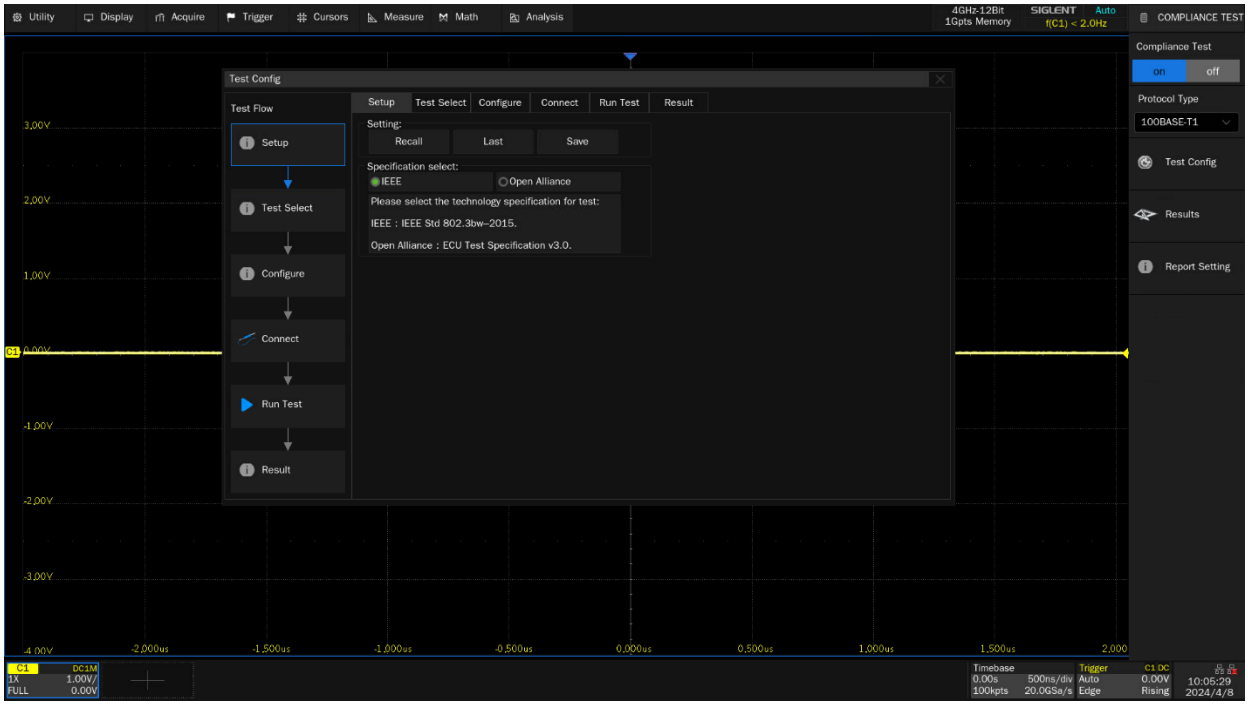


Figure 4-2 Test configuration window

➢ **Test Select**: Select the items to be tested in this tab, which is shown in Figure 4-3.

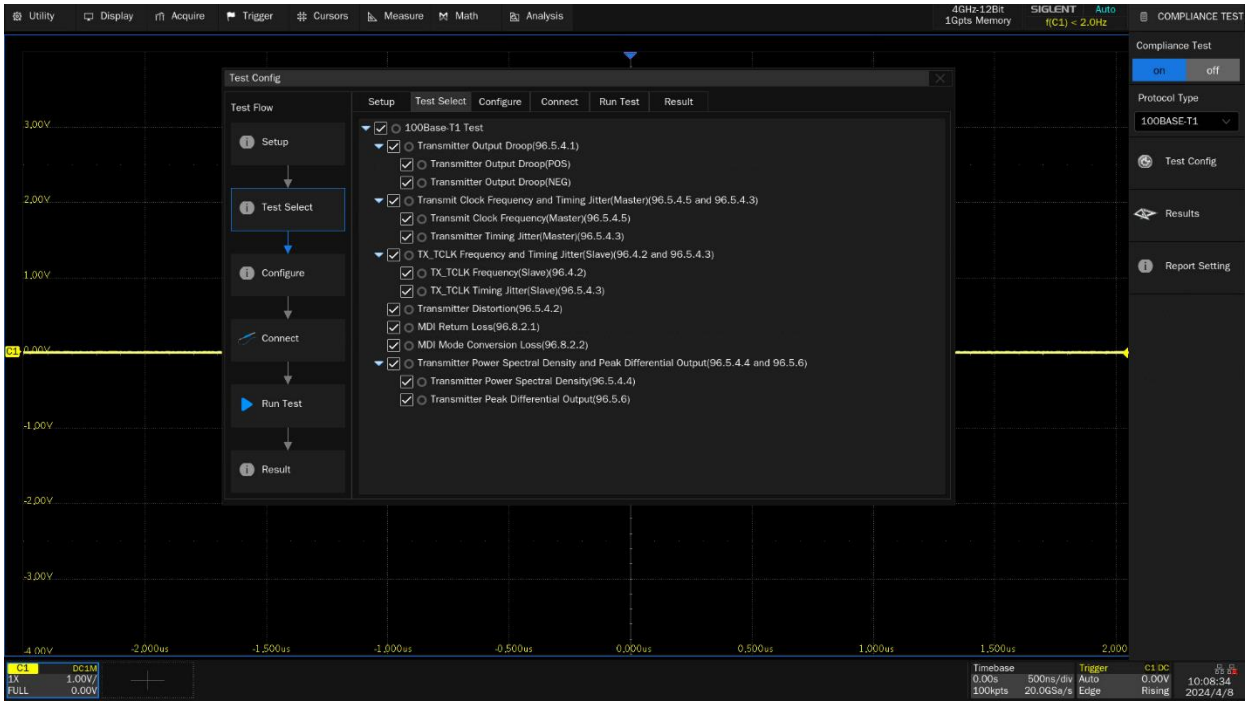


Figure 4-3 Test items selection window

➢ **Configure**: The test items selected in **Test Select** tab will be highlighted in this tab, and you can click the corresponding items to configure. You can set the input channels and probe types, average number, which is shown in Figure 4-4.

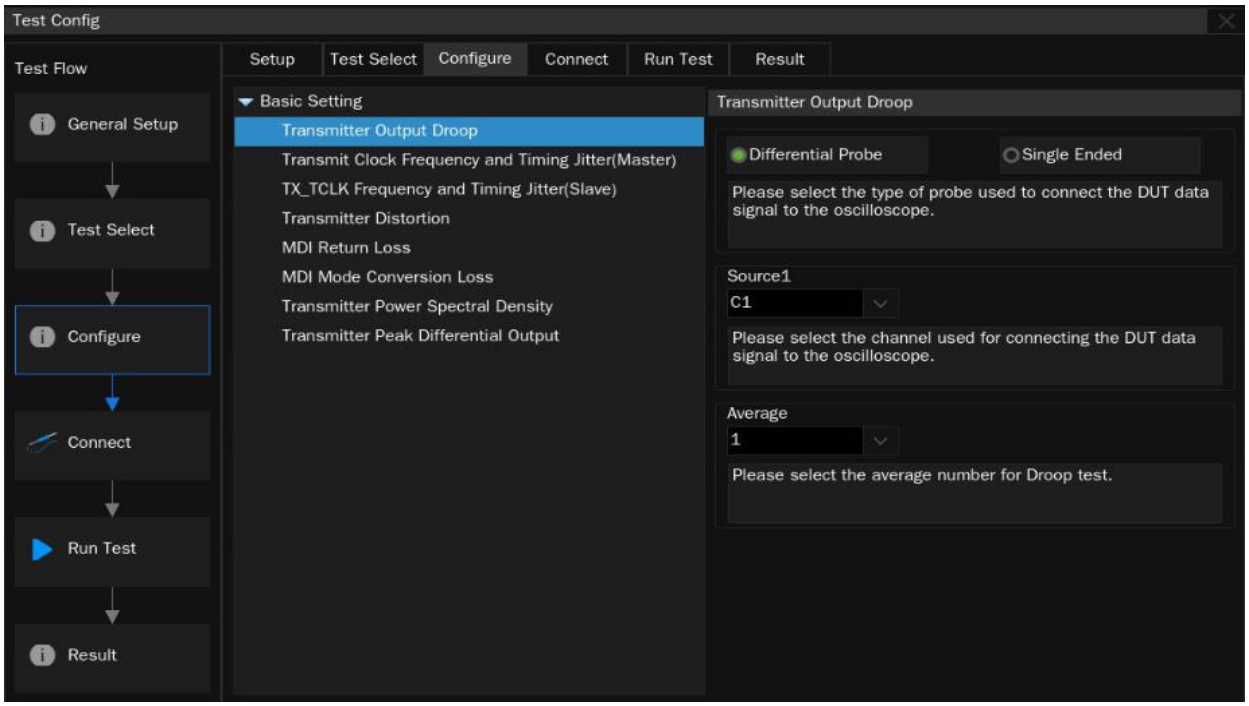


Figure 4-4 Configuration window

- **Connect**: This tab displays the connection diagram of the compliance test, which is shown in Figure 4-5. If more than one item is selected simultaneous, only the connection diagram for the first test item will be displayed. For the other test items, if the connection is different, then a new pop-up window will appear at the end of the previous test.

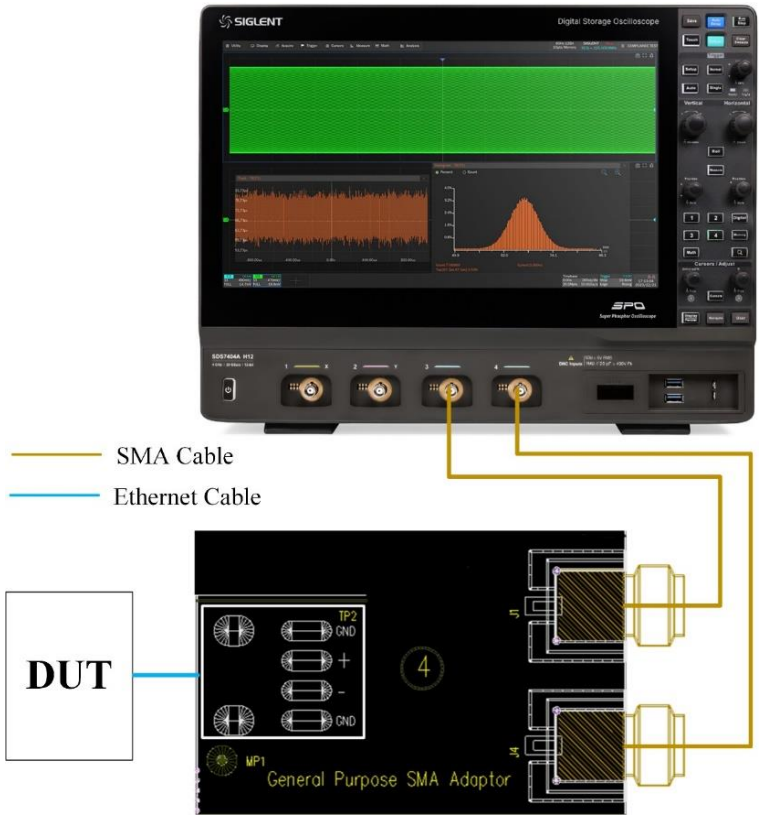


Figure 4-5 Connection diagram displayed in the Connect tab

- **Run Test:** The Run Test window is shown in Figure 4-6. Both **Continue** and **Stop** options are supported when meets test failures.

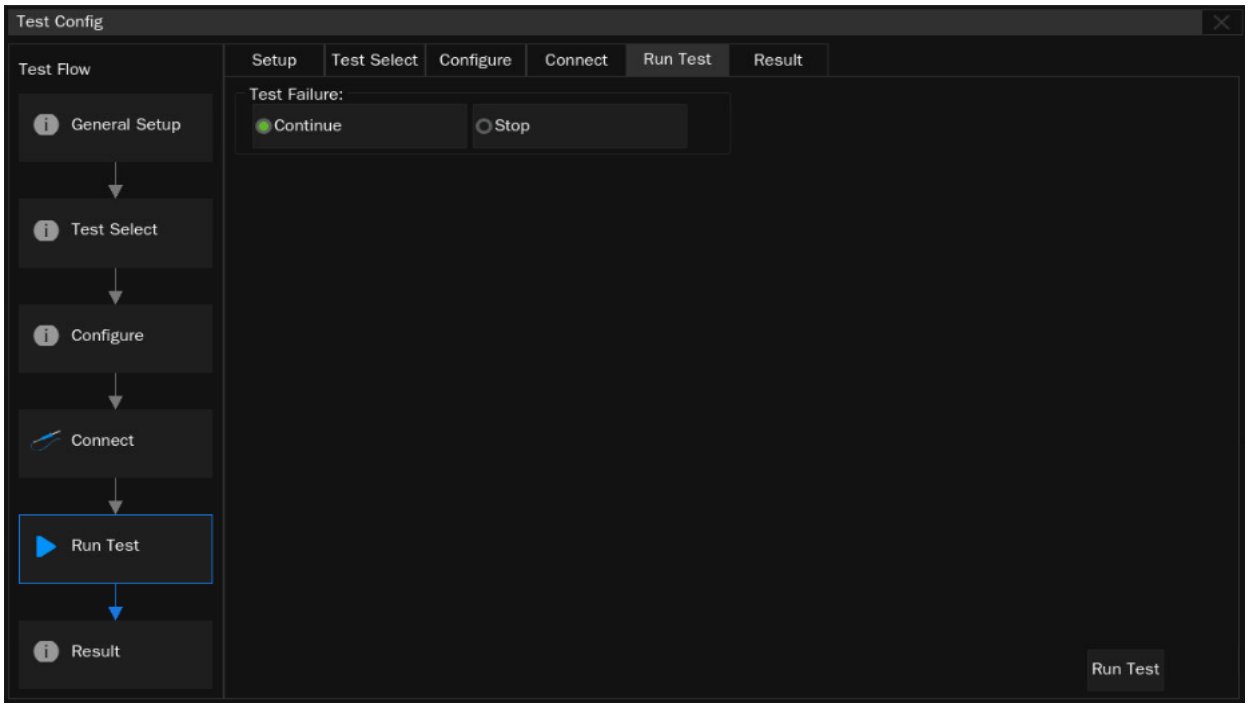


Figure 4-6 Run Test window

In the following test process, according to the pop-up window prompts to complete the test. After all test items are completed, the test result window will pop up.

If more than one test item is selected in a round of tests, if there are different connection methods, there will be a pop-up window at the end of the previous test to prompt the connection method of the current test item before the test run is carried out, after changing the connection environment, click **Run Test** in the pop-up window to continue the test run.

4.2 View Test Results

Click **Result** to view the corresponding test results.

The upper half of the test results window contains the test items, outlining the results of every test item, as well as the pass thresholds, which is shown in Figure 4-7.

The lower half of the test result window is the corresponding detail waveform, click on the item you are concerning in the upper half of the test results window, and the corresponding details will be displayed in the lower half of the window, click on the picture to see the details of the test waveform in a large view, as shown in Figure 4-8.

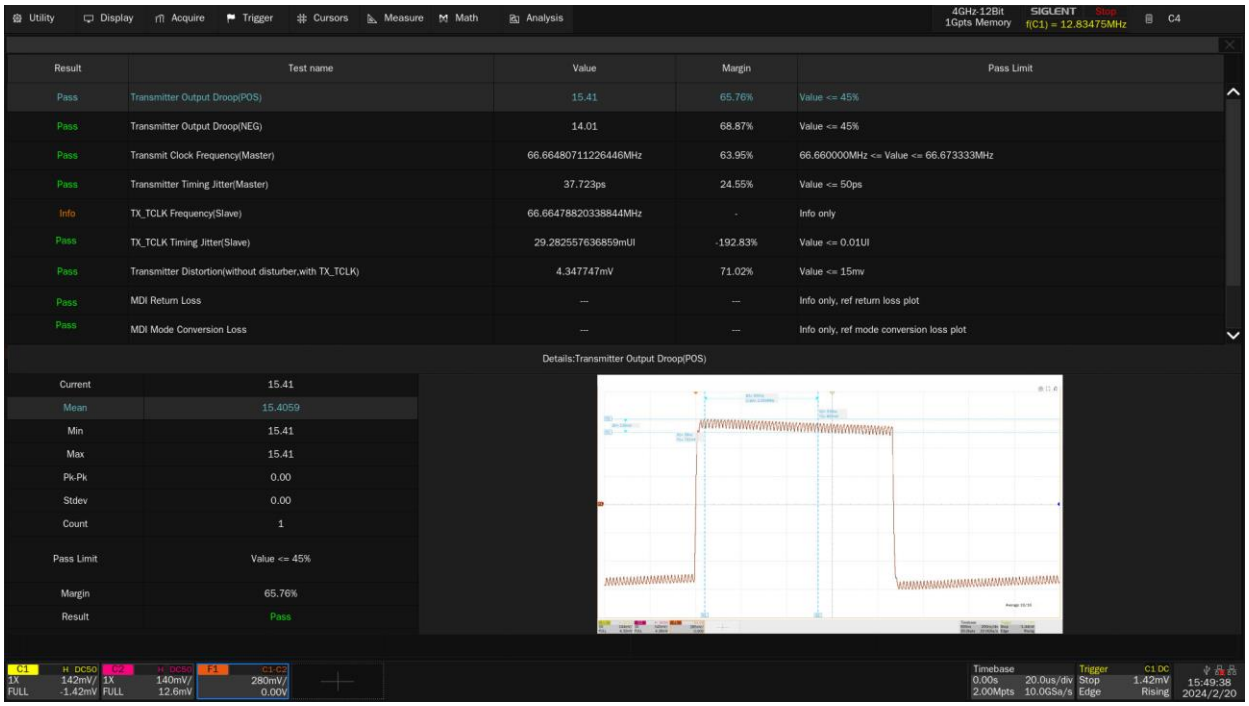


Figure 4-7 List of test result items

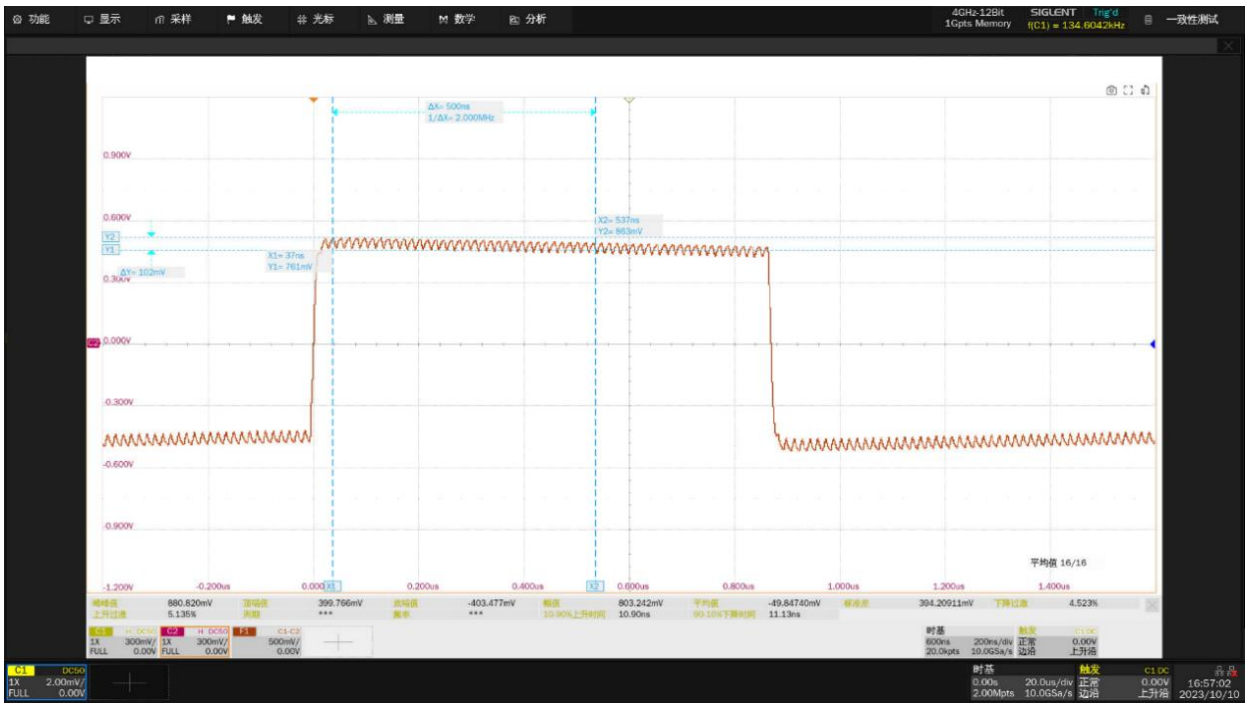


Figure 4-8 Waveform details

4.3 Report Generation

Click **Report Setting** , fill in the test information, and select the HTML or XML report type to generate. **Preview Report** can view the generated report in advance. Click **File Management** to select the path to save. Click **Save** to save the test results, as shown in Figure 4-9.

Note: When saved in HTML format, a folder and a HTML file will be generated, if you need to copy the report to a new directory, you need to copy both files to the new directory.

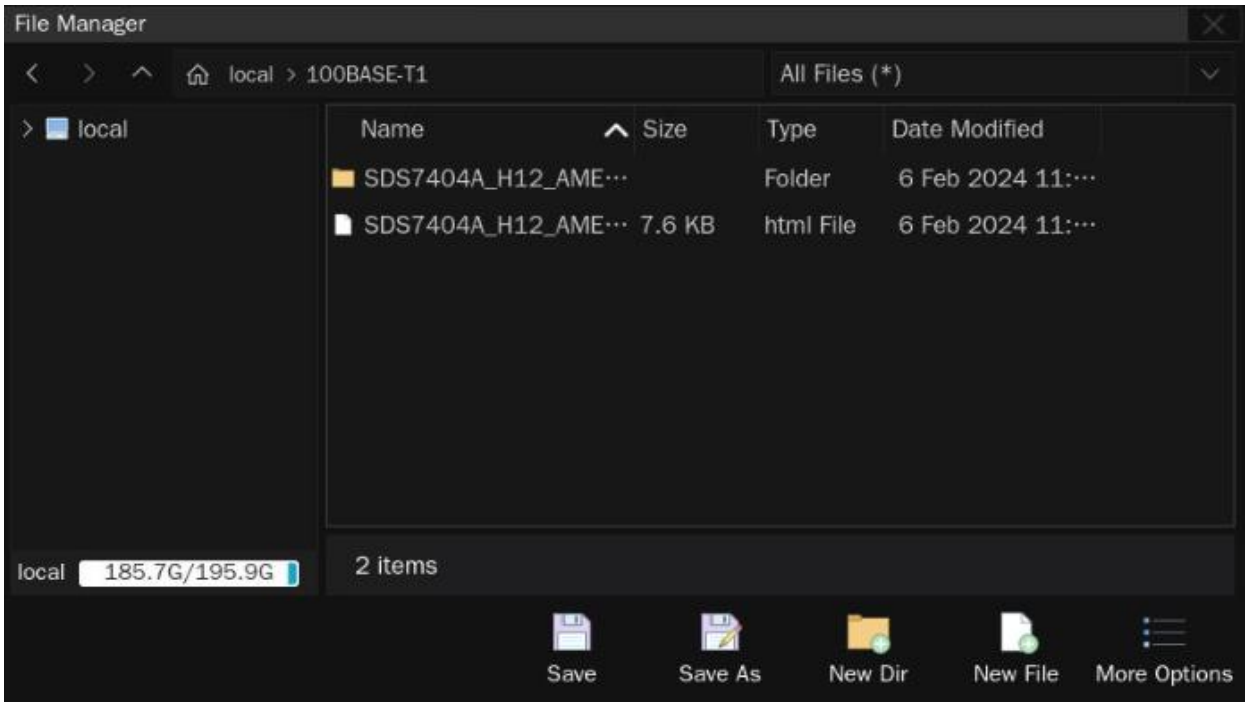


Figure 4-9 Generation of report settings

The test report includes a summary table of all test results and with hyperlinks to the details page, the details page includes a screen shot of the associated test waveform, as shown in Figure 4-10.

SIGLENT®

Automotive Ethernet 100base-T1 Compliance Test Reoprt

Overall Result: Pass

Operator:	
Test Date:	2024-03-19 14:35:39
Device:	
Temperature:	
Remarks:	
Oscilloscope Name:	SDS7404A H12
Oscilloscope Serial Number:	SDS7AA0D789058
Oscilloscope Scope ID:	7544-a623-949f-8aa0
Oscilloscope Firmware Version:	04.13.01.1.1.5.1_20200
Test Result:	Total:2,Pass:2,Not Tested:0,Fail:0

Summary

Result	Test name	Value	Value(Min)	Value(Max)	Margin	Pass Limit
PASS	Transmitter Output Droop(POS)	11.12	11.12	11.12	75.30%	Value <= 45%
PASS	Transmitter Output Droop(NEG)	12.30	12.30	12.30	72.66%	Value <= 45%

Details

[Top]

Transmitter Output Droop(POS)	
Current	11.12
Mean	11.1152
Min	11.12
Max	11.12
Pk-Pk	0.00
Stdev	0.00
Count	1
Pass Limit	Value <= 45%
Margin	75.30%
Result	PASS

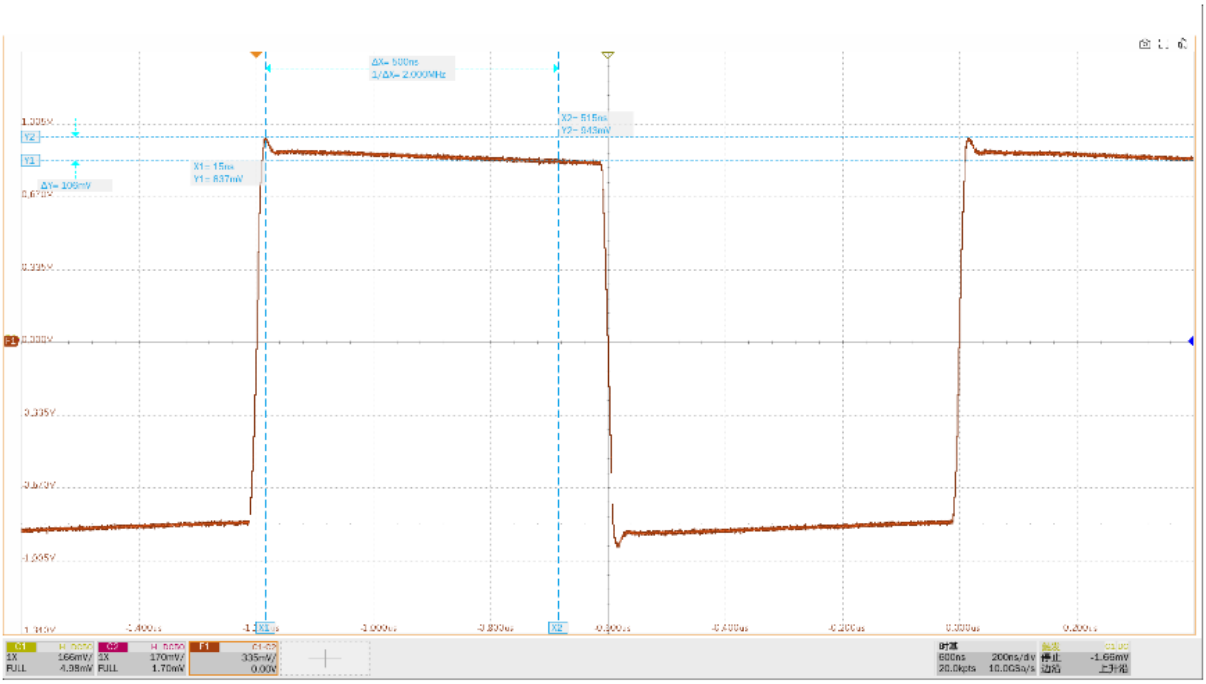


Figure 4-10 An example of the test report

5 100BASE-T1 Compliance Tests

5.1 Transmitter Output Droop Tests

When test mode 1 is enabled, the PHY shall transmit N “+1” symbols followed by N “–1” symbols. The value of N shall be a minimum of 34 symbol periods to achieve a symbol period greater than 500 ns. This sequence is repeated continually. For example, a PHY with test mode 1 enabled and N = 40 symbols (symbol period of 600 ns) would transmit a pattern sufficiently long enough for a 500 ns droop measurement.

A typical output waveform of test mode 1 by the DUT is shown in Figure 5-1.

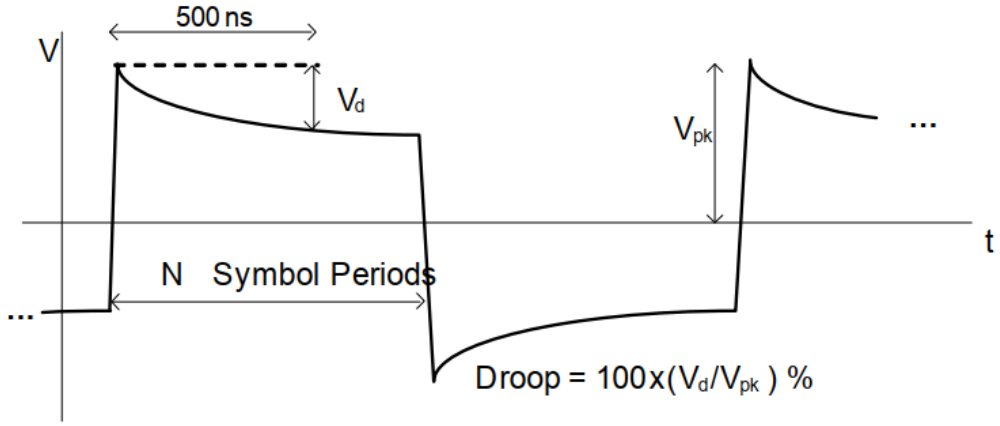


Figure 5-1 The output waveform of Test Mode 1

5.1.1 Test Environment and Connectivity

A pair of SMA cables or an active differential probe can be used to probe the signal.

The connection by using a pair of SMA cables is shown in Figure 5-2. The connection procedure is as follows:

(1) Use two SMA cables with equal length to connect the test points J1(+) and J4(-) on section ④ of the test fixture, and to two input channels which are selected as the DUT “Source” channels in the user interface’s **Configure** tab.

(2) Solder the Ethernet cable of the DUT to TP2 on the test fixture.

(3) A cable tie can be used to fasten the Ethernet cable to the through-hole.

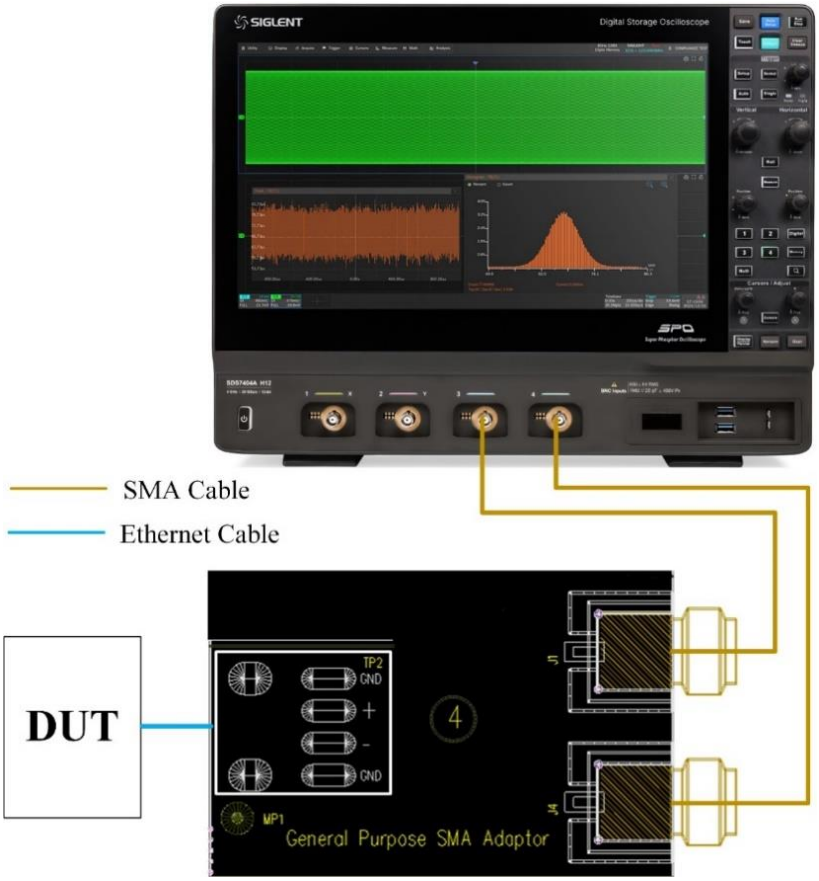


Figure 5-2 Connection to the Oscilloscope by using a pair of SMA cables

The connection by using an active differential probe is shown in Figure 5-3. The connection procedure is as follows:

(1) Connect an active differential probe to the test point J17 on section ① of the test fixture, and to the Oscilloscope input channel which is selected as the DUT "Source" channel in the user interface's **Configure** tab.

(2) Solder the Ethernet cable of the DUT to TP4 on the test fixture.

(3) Ensure correct polarity of the probe head.

(4) A cable tie can be used to fasten the Ethernet cable to the through-hole.

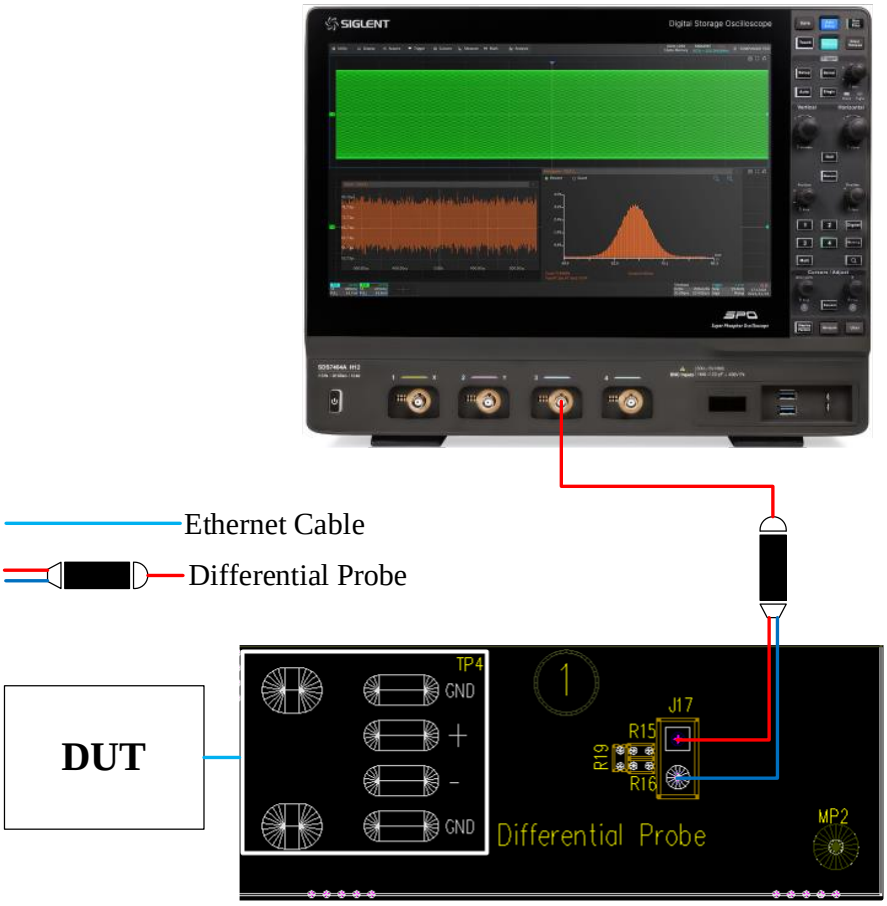


Figure 5-3 Connection to the Oscilloscope by using a Differential Probe

5.1.2 Test Procedure

(1) Configure the DUT to output test mode 1 signal.

(2) Select **IEEE** or **OPEN Alliance** specification for the compliance test in **Setup** tab.

(3) Select the **Transmitter Output Droop** In the **Test Select** tab.

(4) Set the probe type (differential probe or single-ended input), source channel and average number in the **Configure** tab.

(5) Check the correctness of the test environment setup in the **Connect** tab.

(6) Click **Run Test** .

(7) If the system is not physically configured to perform this test, the application will return to the **Connect** step to prompt you to change the physical configuration. When you have completed these instructions, click **Run Test** button to resume the test run.

(8) During the test, the Oscilloscope will automatically verify whether the correct test signal is present on the configured DUT “Source” channel, if effective signal is detected, the Oscilloscope will configure the correct trigger level to capture the signal. After finishing the tests, the Oscilloscope will output the test results.

5.1.3 Algorithm

The transmitter output droop is measured according to the section 96.5.4.1 of IEEE Std 802.3bw specification, and the section OABR_PMA_TX_01 of TC8 ECU specification from OPEN Alliance. The positive and negative droop measured with the initial peak value after the zero-crossing and the value at 500ns after the initial peak, the droop value shall be less than 45%.

The Oscilloscope triggers the Test Mode 1 signal on the rising edge and falling edge and determines the time where the peak voltage occurred and the peak voltage at that specific instance. And then measures the voltage at 500ns after the peak. The droop is calculated as follows:

$$\text{Droop} = 100\ \% \times (Vd/Vpk)$$

Where Vpk is the initial peak level amplitude after zero-crossing, and Vd is the magnitude of the droop at 500ns after the initial peak level.

5.1.4 Test Results Reference

The transmitter output droop test results are shown in Figure 5-4.

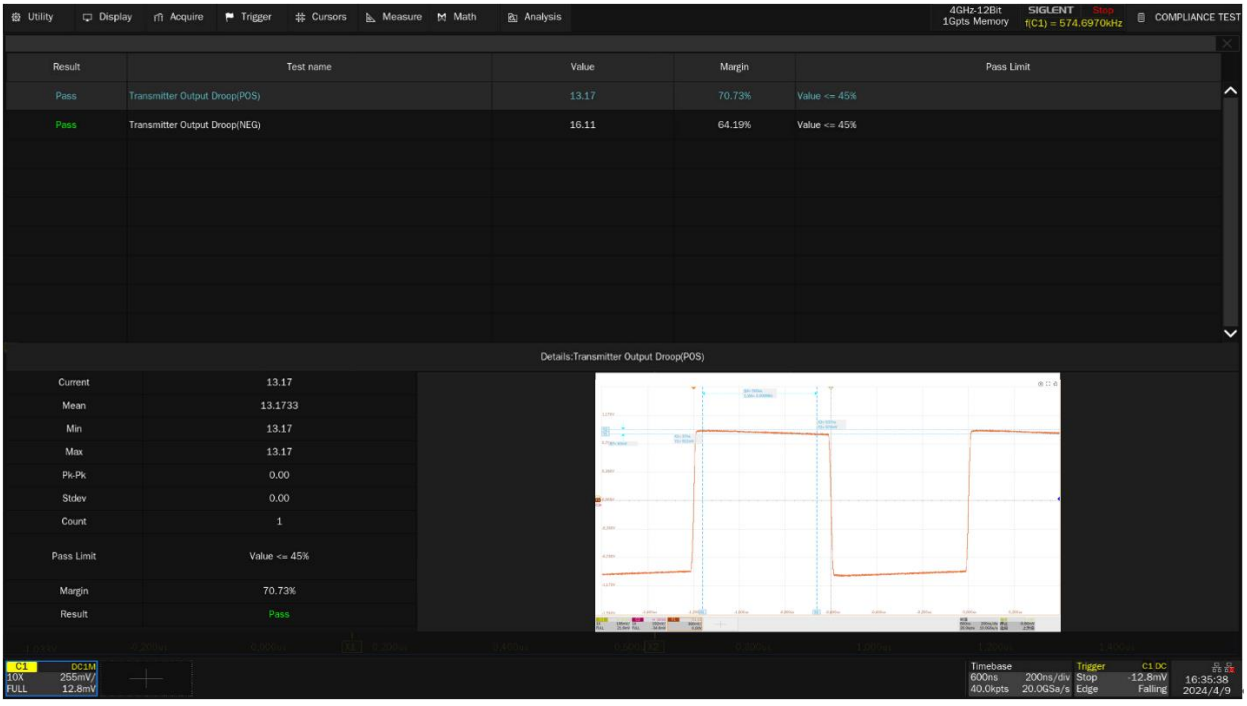


Figure 5-4 Test results of transmitter output droop

The details of the test waveform for transmitter output droop (positive edge) are shown in Figure 5-5.

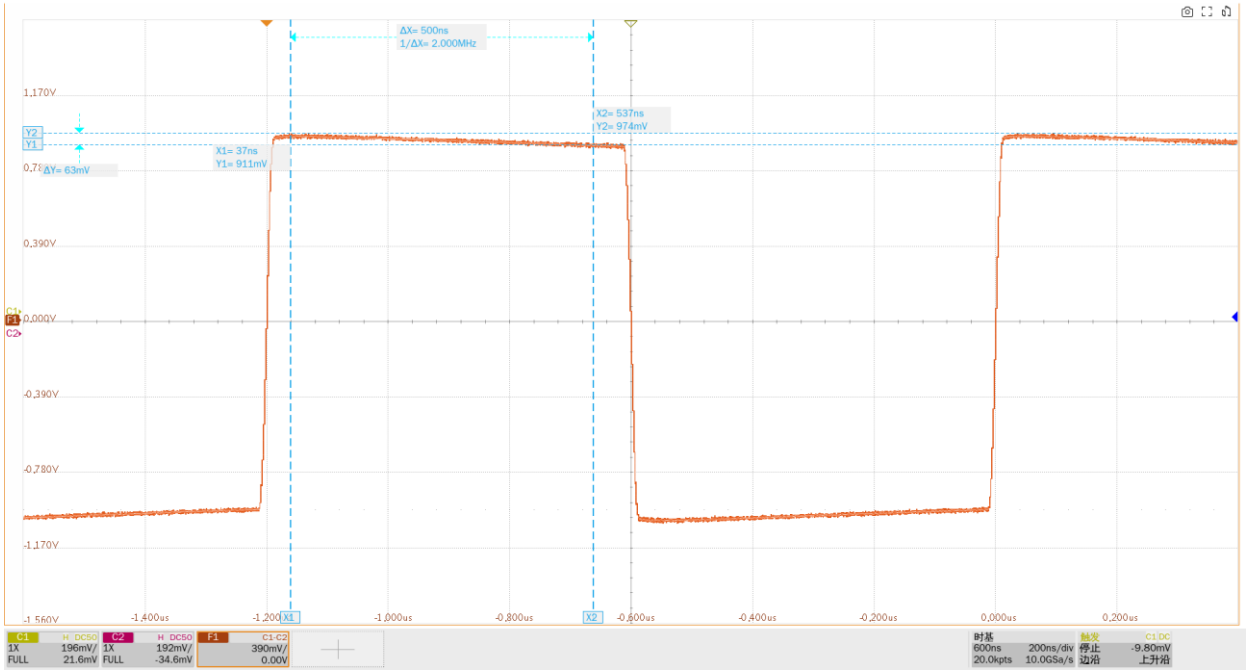


Figure 5-5 Waveform details for positive edge droop test of the transmitter

5.2 Transmit Clock Frequency and Transmitter Timing Jitter Tests (Master Mode)

These test items measure the physical layer transmit clock frequency and transmitter timing jitter when DUT is in Master mode.

In these tests, we need to measure the output waveform of test mode 2 from the DUT, following the IEEE 802.3bw and OPEN Alliance specifications, the transmitter periodically sends out “+1” and “-1” data symbols using a clock of $66^2/_3$ MHz±100 ppm (i.e., 66.6603MHz~66.6736MHz) in the Master mode, the Oscilloscope will measure the symbol rate and transmitter timing jitter.

5.2.1 Test Environment and Connectivity

Test environment and connection for transmit clock frequency and transmitter jitter tests are the same as <5.1.1Test Environment and Connectivity> chapter.

The test environment and connection by using a pair of SMA cables is shown in Figure 5-2.

The test environment and connection by using an active differential probe is shown in Figure 5-3.

5.2.2 Test Procedure

(1) Configure the DUT to output test mode 2 signal.

(2) Select **IEEE** or **OPEN Alliance** specification for the compliance test in **Setup** tab.

(3) Select the **Transmit Clock Frequency and Transmitter Timing Jitter(Master)** In the **Test Select** tab.

(4) Set the probe type (differential probe or single-ended input), source channel, edge and average number in the **Configure** tab.

(5) Check the correctness of the test environment setup in the **Connect** tab.

(6) Click **Run Test** .

(7) If the system is not physically configured to perform this test, the application will return to the **Connect** step to prompt you to change the physical configuration. When you have completed these instructions, click **Run Test** button to resume the test run.

(8) During the test, the Oscilloscope will automatically verify whether the correct test signal is present on the configured DUT “Source” channel, if effective signal is detected, the Oscilloscope will configure the correct trigger level to capture the signal. After finishing the tests, the Oscilloscope will output the test results.

5.2.3 Algorithm

The transmit frequency and transmitter timing jitter is measured according to the section 96.5.4.5 of IEEE Std 802.3bw specification, and the section OABR_PMA_TX_03 of TC8 ECU specification from OPEN Alliance, these specifications specify that the symbol transmission rate for compliance in the Physical Layer.

When test mode 2 is enabled, the PHY shall transmit the data symbol sequence {+1, –1} repeatedly on its channel. The transmitter shall time the transmitted symbols from a 66.666 MHz ± 100 ppm clock in the Master timing mode.

Therefore, the measured data symbol rate to Test Mode 2 is equal to the PHY's transmit clock frequency in Master mode.

The section 96.5.4.3 of IEEE Std 802.3bw specification, and the section OABR_PMA_TX_02 of TC8 ECU specification from OPEN Alliance specify that when the DUT is in Test Mode 2, the DUT's MDI output RMS (RMS, Root Mean Square) jitter, JTXOUT, relative to the jitter-free reference, shall be less than 50 ps. Transmitter timing jitter measures the data time interval error (TIE) of the test mode 2 signal on the MDI. The Oscilloscope automatically selects the ideal reference clock and compares it to the original signal to determine the time interval error.

5.2.4 Test Results Reference

The transmit clock frequency and transmitter timing jitter test results are shown in Figure 5-6.

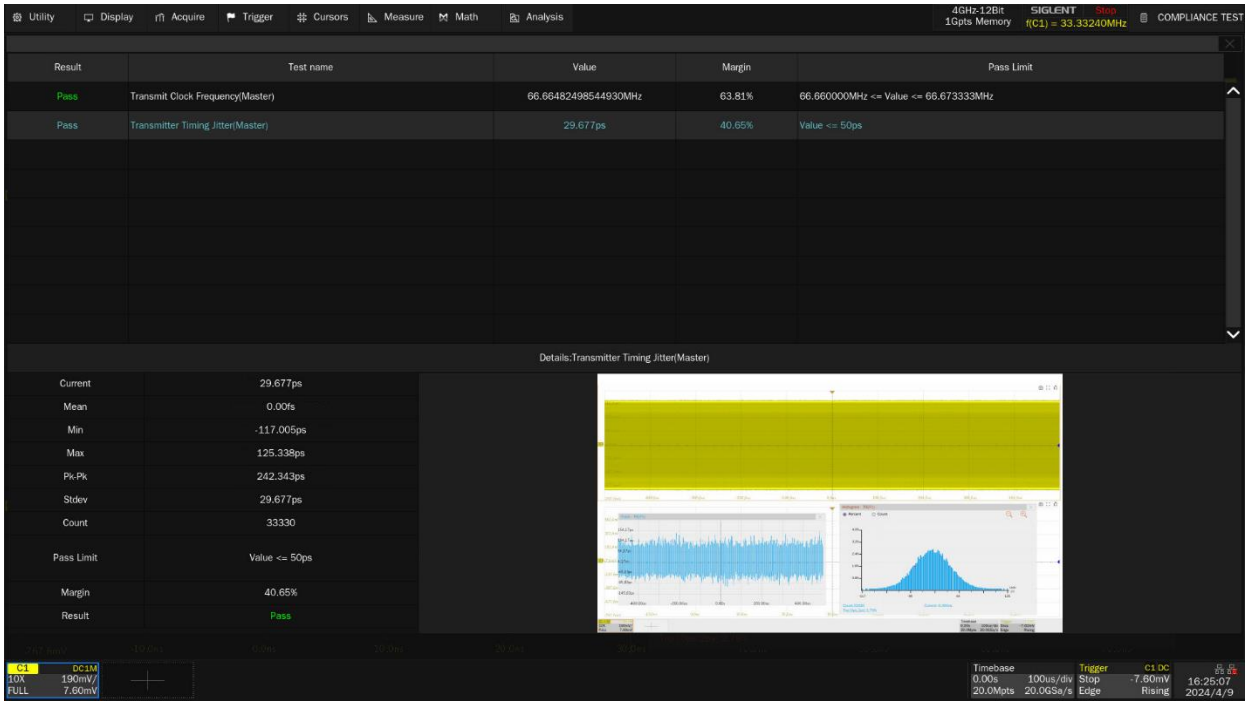


Figure 5-6 Test results of Test Mode 2

The details of the test waveform for transmitter timing jitter test are shown in Figure 5-7.

Figure 5-7 Waveform details for transmitter timing jitter test

5.3 TX_TCLK Frequency and Timing Jitter Tests (Slave Mode)

These test items measure the physical layer transmit clock frequency and transmitter timing jitter when DUT is in Slave mode. The DUT needs to provide TX_TCLK signal for compliance test.

The specification of IEEE Std 802.3bw, section 96.5.4.5 specifies data symbol rate of the Master PHY shall be in the range of 66 2/3 MHz±100ppm.

Although the IEEE Std 802.3bw standard does not specify the conformance limit when the DUT is in Slave mode, the symbol rate in Slave mode should be the same as the Master PHY, which is 66 $^{2}/_{3}$ MHz.

Section 96.5.4.3 of the IEEE Std 802.3bw specification specifies that the RMS value of the Slave TX_TCLK jitter relative to an unjittered reference shall be less than 0.01 UI (Unit Interval) after the receiver is properly receiving the data.

5.3.1 Test Environment and Connectivity

According to Figure 96-24 in Section 96.5.4.3 of the IEEE Std 802.3bw specification, the test should connect the DUT(Slave) to the Link Partner (Master) with an Ethernet cable, both of Link Partner and DUT are in normal operation mode, which is shown in Figure 5-8. The TX_TCLK clock of the DUT is directly connected to the input channel of Oscilloscope.

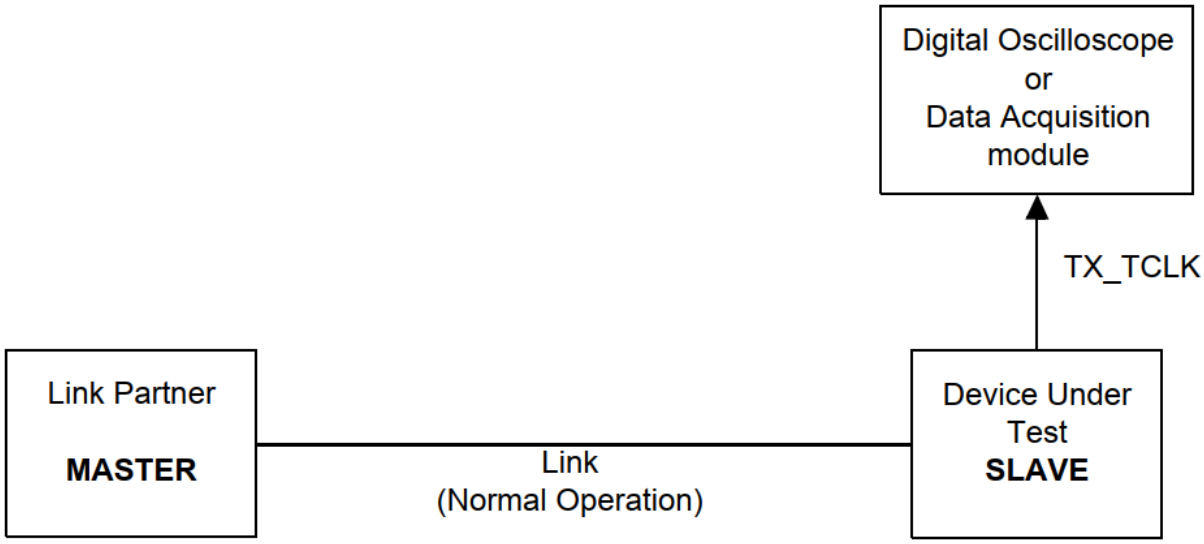


Figure 96–24—Setup for slave transmit timing jitter in normal mode

Figure 5-8 Test environment and connectivity for TX_TCLK when the DUT is in Slave mode

On SDA7000A, the test environment and connection for TX_TCLK frequency and jitter tests when the DUT is in Slave mode is shown in Figure 5-9.

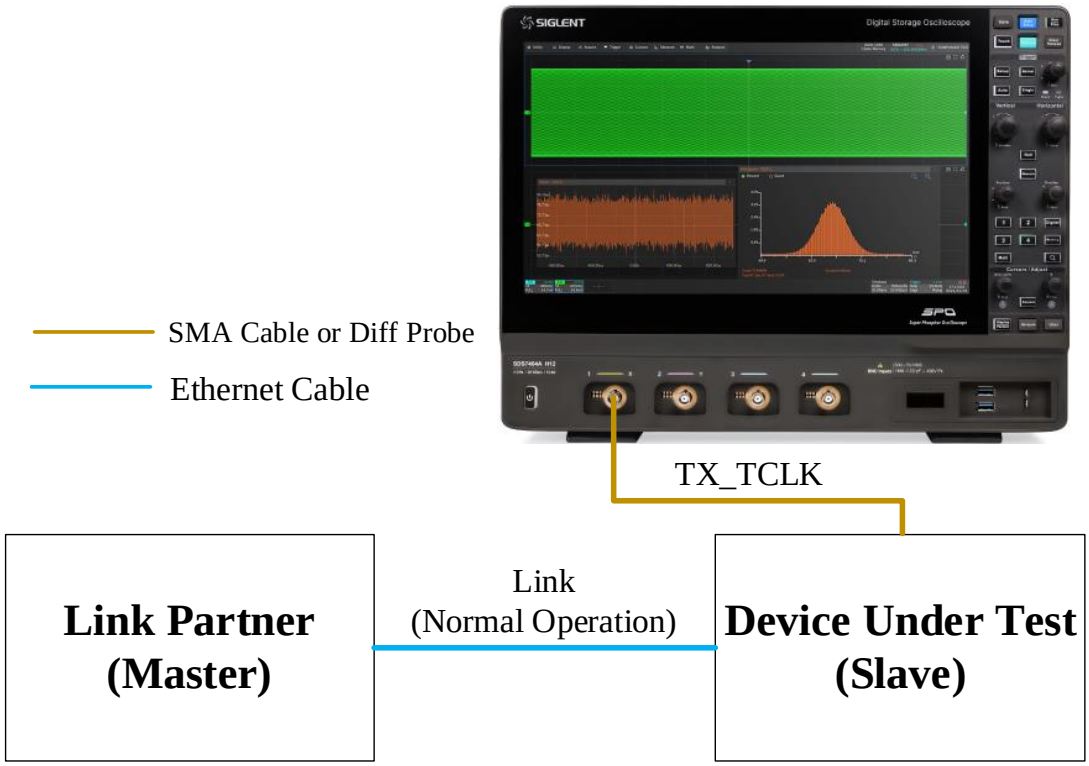


Figure 5-9 Connection of TX_TCLK when DUT is in Slave mode

5.3.2 Test Procedure

(1) Configure the DUT to Slave mode, and the Link Partner is set as the Master. The link between Link Partner and DUT is in normal operation.

(2) Select **IEEE** specification for the compliance test in **Setup** tab.

(3) Select the **TX_TCLK Frequency and Timing Jitter(Slave)** In the **Test Select** tab.

(4) Set the source channel, input impedance, average number and edge in the **Configure** tab.

(5) Check the correctness of the test environment setup in the **Connect** tab.

(6) Click **Run Test** .

(7) If the system is not physically configured to perform this test, the application will return to the **Connect** step to prompt you to change the physical configuration. When you have completed these instructions, click **Run Test** button to resume the test run.

(8) During the test, the Oscilloscope will automatically verify whether the correct test signal is present on the configured DUT “Source” channel, if effective signal is detected, the Oscilloscope will configure the correct trigger level to capture the signal. After finishing the tests, the Oscilloscope will output the test results.

5.3.3 Algorithm

The transmit frequency is measured according to the specification of IEEE Std 802.3bw, section 96.5.4.5, the symbol transmission rate for the Master is 66.666 MHz ± 100 ppm.

Although the IEEE Std 802.3bw standard does not specify the conformance limit when the DUT is in Slave mode, the symbol frequency in Slave mode should be the same as the Master PHY, which is 66 $^{2}/_{3}$ MHz.

The specification of IEEE Std 802.3bw, section 96.5.4.3, specifies that the RMS value of the SLAVE TX_TCLK jitter relative to an unjittered reference shall be less than 0.01 UI (Unit Interval) after the receiver is properly receiving the data. The TX_TCLK jitter measures the TX_TCLK time interval error (TIE). The Oscilloscope automatically selects the ideal reference clock and compares it to the original signal to determine the time interval error.

5.3.4 Test Results Reference

The TX_TCLK clock frequency and timing jitter test results are shown in Figure 5-10.

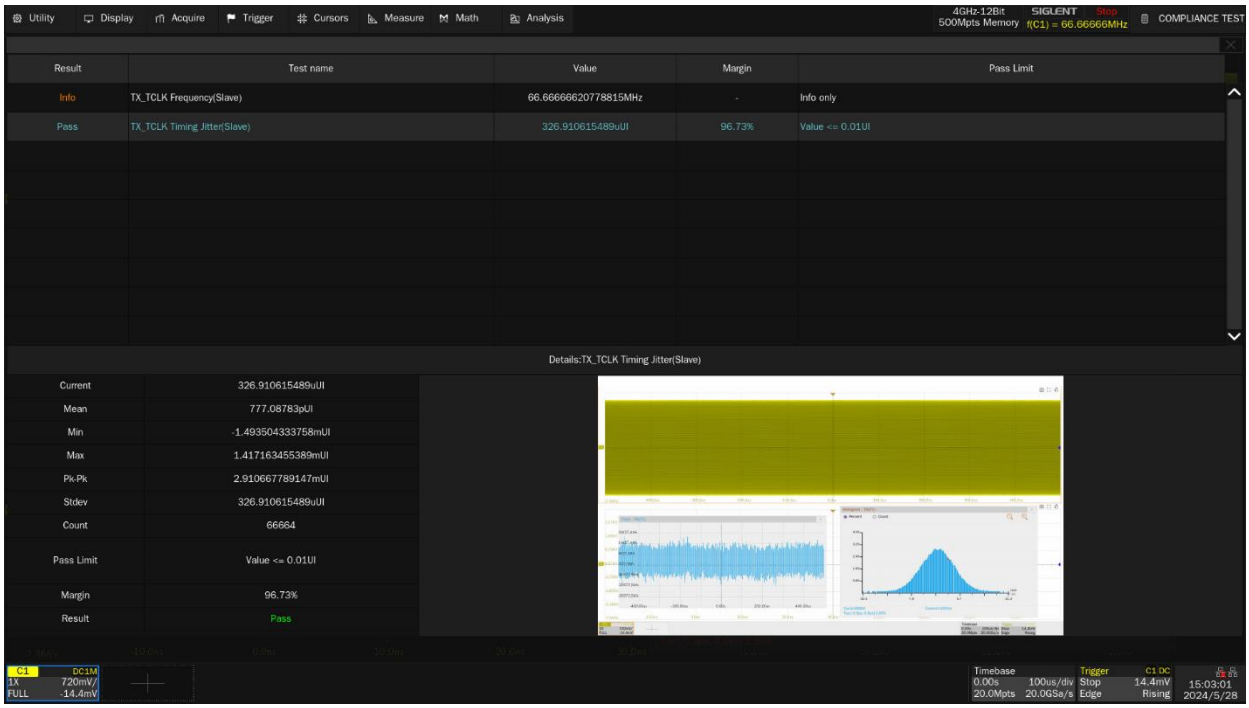


Figure 5-10 Test results of TX_TCLK frequency and timing jitter

The details of the test waveform for TX_TCLK timing jitter test are shown in Figure 5-11.

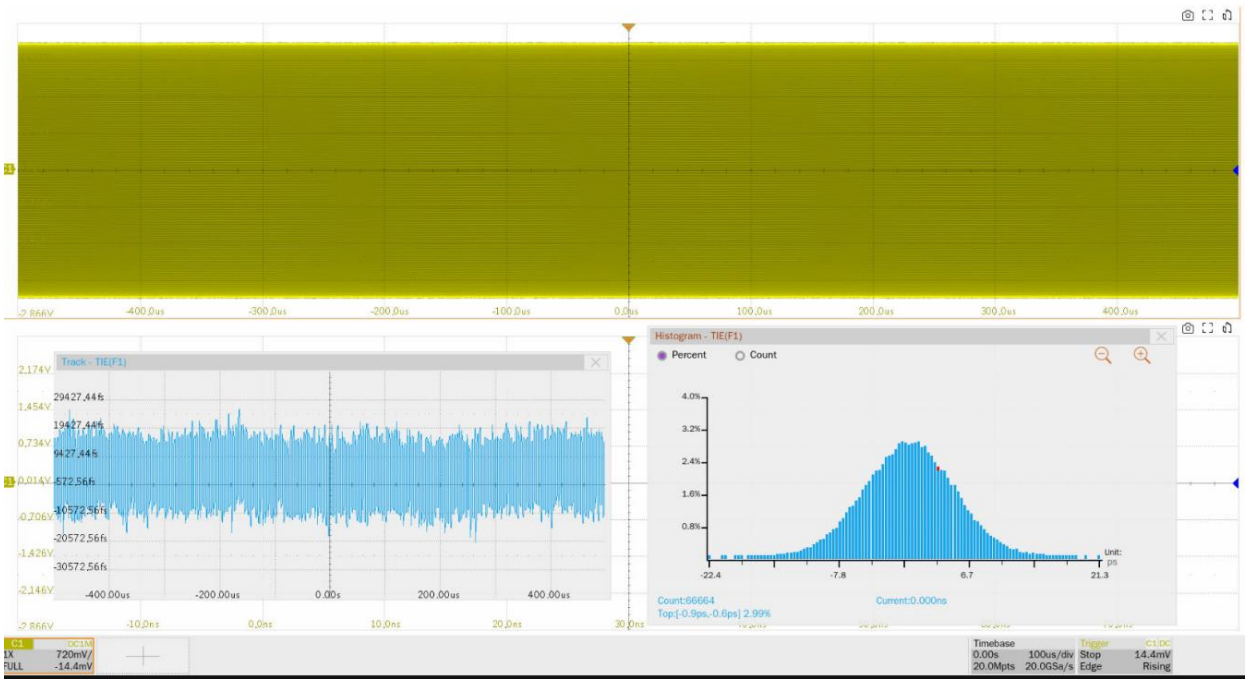


Figure 5-11 Waveform details for TX_TCLK timing jitter test

5.4 Transmitter Distortion Test

The transmitter distortion test is according to the section 96.5.4.2 of IEEE Std 802.3bw specification, and the section OABR_PMA_TX_08 of TC8 ECU specification from OPEN Alliance. The DUT continuous sends out many blocks of 2047 defined symbols after it enters into test mode 4. Section 96.5.4.2 of IEEE Std 802.3bw specification provides MATLAB code to analyze transmission distortion.

5.4.1 Test Environment sand Connectivity

The configuration of the transmitter distortion on the SDS7000A Oscilloscope is shown in Figure 5-12. Siglent's transmitter distortion test supports the use of Arbitrary Waveform Generator to output disturbing signals to the DUT for distortion test.

Alternatively, you can also run distortion test without the disturbing signal, but you cannot use the result to determine compliance. By this way, the user can uncheck the **Disturbing Signal** to do the transmitter distortion test.

In order to improve the accuracy of transmitter distortion test, you need to check **TX_TCLK** in the configure tab. Then connect **TX_TCLK** of the DUT to the input connector(J1 or J2) of the Frequency Converter test fixture, the test fixture will generate two identical 10MHz clock signals from TX_TCLK, both of the 10MHz clock output needed to connect to the external clock source ports of the Oscilloscope and the Disturber. By this way the clock domain synchronization among the DUT,

Oscilloscope and Arbitrary Waveform Generator can be achieved.

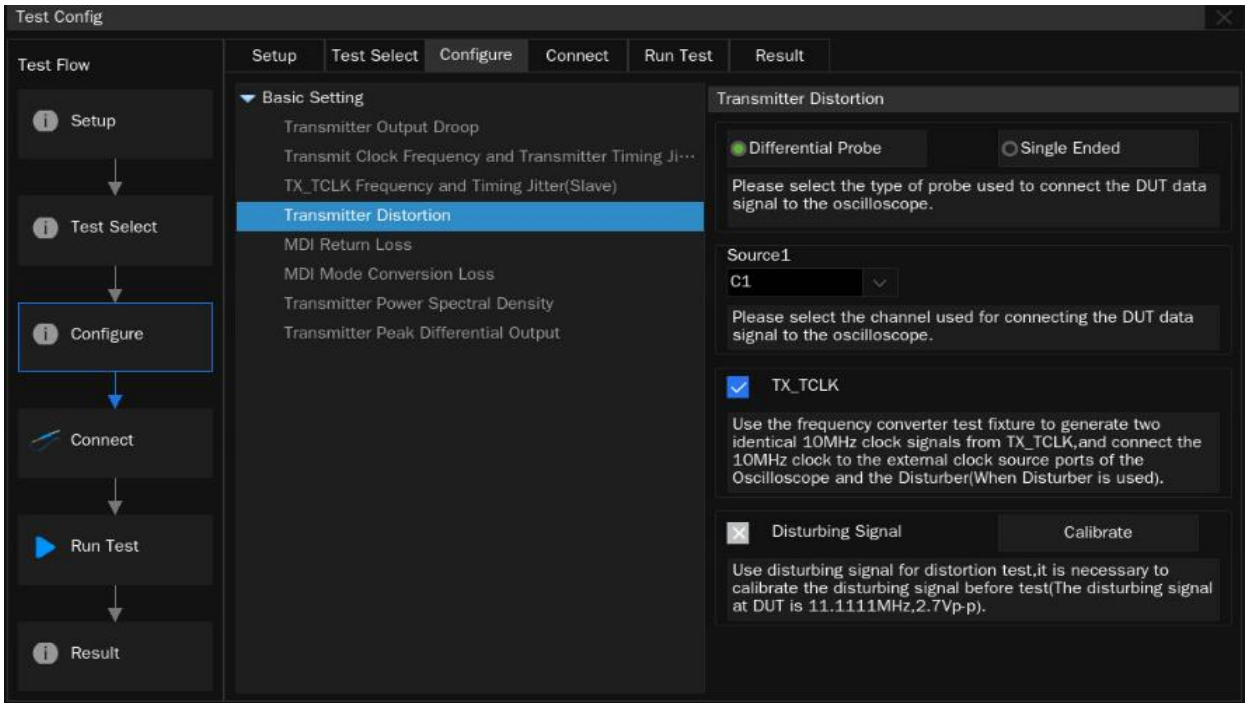


Figure 5-12 The configuration of transmitter distortion test

5.4.1.1 Disturbing Signal Path Calibration

After checking **TX_TCLK** and **Disturbing Signal**, it is necessary to calibrate the disturbing signal before performing the transmitter distortion test, the calibration environment and connection is shown in Figure 5-13. The calibration procedure for disturbing signal path is as follows:

(1) The connection between Frequency Converter and test equipment is as follows:

1) Supply a DC5V power to the Frequency Converter test fixture through J6 or J9 connector, the HL3 and HL5 LED will light up.
2) Connect the DUT's TX_TCLK to the J1(CH1) or J2(CH2) input channel on the Frequency Converter test fixture. Install a jumper on J5(pin 1,2) to select CH2 as the input channel (CH2 input impedance is 50ohm); Install a jumper on J5(pin 2,3) to select CH1 as the input channel (CH1 input impedance is 10kohm).
3) Input clock frequency selection: place the jumper on J7(pin1,2) to indicates the input clock frequency of TX_TCLK is 66.667MHz.
4) Check the frequency lock indicator: When HL1 lights up, which means that the frequency conversion from 66.667MHz to 10MHz works well. When HL1 is off, it means that the PLL chip is not locked, you need to check whether the input clock, J5 and J7 are configured correctly or not. When the configuration is correct, you can press the Reset Button S1 or power up the Frequency Converter again.
5) Connect J3(Clock Output: CH1) and J12(Clock Output: CH2) to the external clock source

ports of the Oscilloscope and Arbitrary Waveform Generator respectively.

6) Set the clock source of the Oscilloscope and Arbitrary Waveform Generator to external.

(2) Use section ② on the Automotive Ethernet Test Fixture to do the disturbing signal calibration. The connection is shown as follows:

1) J5, J14 connectors are installed with 50ohm terminators.

2) Connect the J2 and J8 connectors on the test fixture to two input channels on the Oscilloscope which are selected as the DUT's "Source" channels in the user interface's **Configure** tab with equal length cables.

3) Connect the J15 and J16 connectors on the test fixture to two output channels on the Disturber.

4) Set the Disturber to output two sine wave signals with the same amplitude but with a 180° phase shift. The sine wave frequency is 11.1111MHz, which is exactly 1/6 of the transmission symbol rate.

5) Set the input impedance of the Oscilloscope to 50Ω. The Oscilloscope subtracts two input signals and measure the peak-to-peak value of the differential signal. Continuously adjust the output amplitude of the Disturber until the peak-to-peak voltage reads to 2.7V_{p-p}. Record and save the Disturber setting for the following transmitter distortion tests.

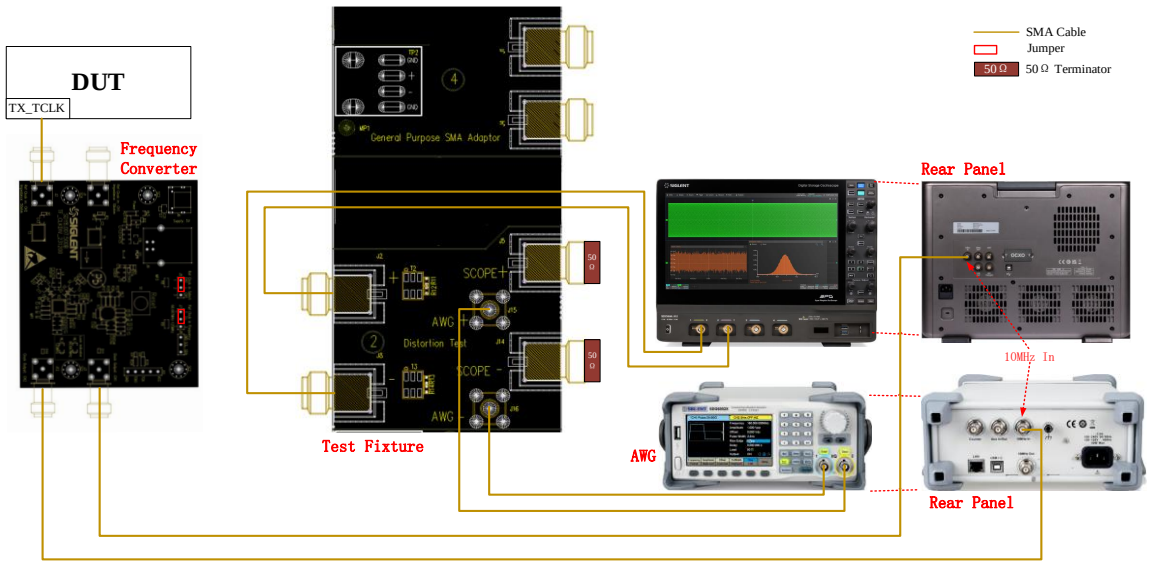


Figure 5-13 Calibration environment and connection for disturbing signal path

5.4.1.2 Environment Setup for Transmitter Distortion Test

The transmitter distortion test can be performed with or without disturbing signal. Please setup the test environment according to requirements. But you cannot use the result to determine compliance without disturbing signal.

A. With TX_TCLK clock and with disturbing signal

The connection with TX_TCLK and with disturbing signal is shown in Figure 5-14. The test procedure is shown as follows:

(1) Configure the DUT to output Test Mode 4 signal.

(2) The connection between Frequency Converter and test equipment is as follows:

1) Supply a DC5V power to the Frequency Converter test fixture through J6 or J9 connector, the HL3 and HL5 LEDs will light up.

2) Connect the DUT's TX_TCLK to the J1(CH1) or J2(CH2) input channel on the Frequency Converter test fixture. Install a jumper on J5(pin 1,2) to select CH2 as the input channel (CH2 input impedance is 50ohm); Install a jumper on J5(pin 2,3) to select CH1 as the input channel (CH1 input impedance is 10kohm).

3) Input clock frequency selection: place the jumper on J7(pin1,2) to indicate the input clock frequency of TX_TCLK is 66.667MHz.

4) Check the frequency lock indicator: When HL1 lights up, which means that the frequency conversion from 66.667MHz to 10MHz works well. When HL1 is off, it means that the PLL chip is not locked, you need to check whether the input clock, J5 and J7 are configured correctly or not. When the configuration is correct, you can press the Reset Button S1 or power up the Frequency Converter again.

5) Connect J3(Clock Output: CH1) and J12(Clock Output: CH2) to the external clock source ports of the Oscilloscope and Arbitrary Waveform Generator respectively.

6) Set the clock source of the Oscilloscope and Arbitrary Waveform Generator to external.

(3) On the section ② and ④ of the Automotive Ethernet Test Fixture. The connection is as follows:

1) Solder the cable of DUT to TP2 on section ④ of the test fixture.

2) On the test fixture, use two SMA cables with equal length to connect the J1(+) and J4(-) connectors on section ④ to J2(+) and J8(-) connectors on section ②.

3) Connect the J15 and J16 connectors on the test fixture to two output channels on the Disturber, with the disturbing sine wave which has been finished calibrating.

4) Connect the J5 and J14 connectors on section ② of the test fixture to two input channels on the Oscilloscope which are selected as the DUT "Source" channels in the user interface's **Configure** tab.

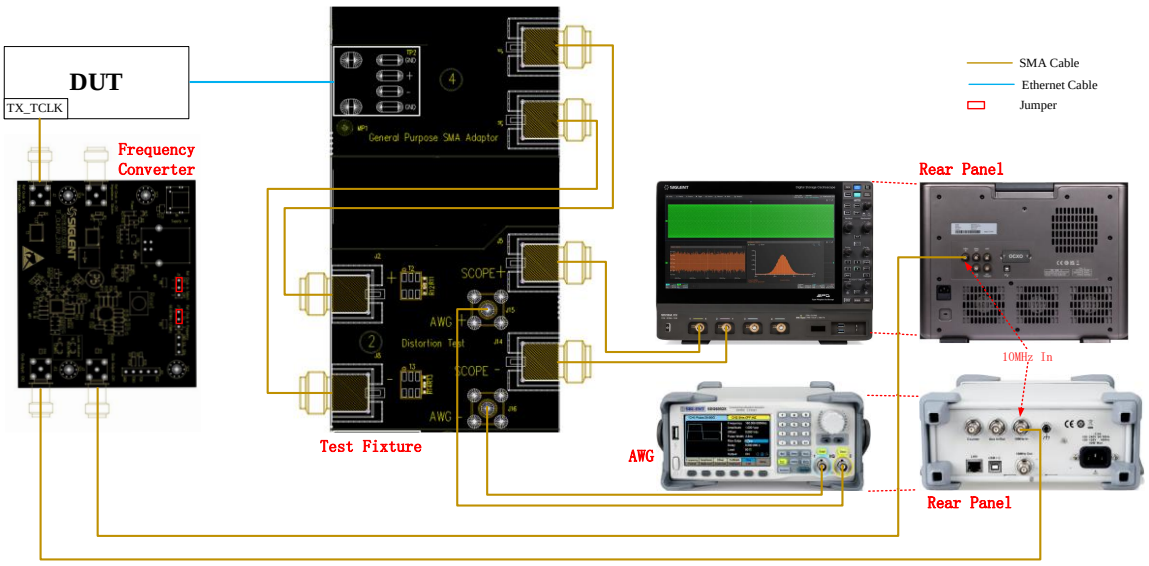


Figure 5-14 Environment setup for transmitter distortion tests by using a pair of SMA cables (with disturbing signal)

B. With TX_TCLK clock, without disturbing signal

(1) Configure the DUT to output Test Mode 4 signal.

(2) The connection between Frequency Converter and test equipment is as follows:

1) Supply a DC5V power to the Frequency Converter test fixture through J6 or J9 connector, the HL3 and HL5 LEDs will light up.

2) Connect the DUT's TX_TCLK to the J1(CH1) or J2(CH2) input channel on the Frequency Converter test fixture. Install a jumper on J5(pin 1,2) to select CH2 as the input channel (CH2 input impedance is 50ohm); Install a jumper on J5(pin 2,3) to select CH1 as the input channel (CH1 input impedance is 10kohm).

3) Input clock frequency selection: place the jumper on J7(pin1,2) to indicate the input clock frequency of TX_TCLK is 66.667MHz.

4) Check the frequency lock indicator: When HL1 lights up, which means that the frequency conversion from 66.667MHz to 10MHz works well. When HL1 is off, it means that the PLL chip is not locked, you need to check whether the input clock, J5 and J7 are configured correctly or not. When the configuration is correct, you can press the Reset Button S1 or power up the Frequency Converter again.

5) Connect J3(Clock Output: CH1) or J12(Clock Output: CH2) to the external clock source port of the Oscilloscope.

6) Set the clock source of the Oscilloscope to external.

(3) On the section ④ of the Automotive Ethernet Test Fixture. The connection is as follows:

1) Solder the cable of DUT to TP2 on section ④ of the test fixture.

2) Use two SMA cables with equal length to connect the J1(+) and J4(-) connectors on section ④ of the test fixture to two input channels on the Oscilloscope which are selected as the DUT "Source" channels in the user interface's **Configure** tab.

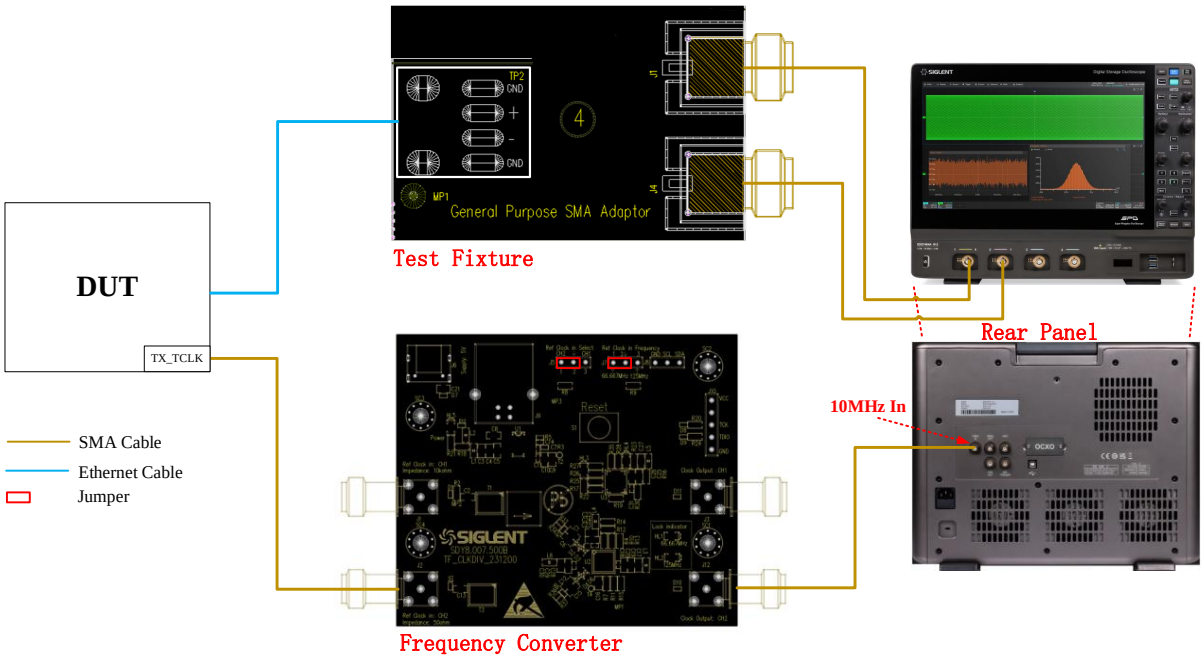


Figure 5-15 Environment setup for transmitter distortion test by using a pair of SMA cables (without disturbing signal)

The test environment and connection for transmitter distortion test with Frequency Converter and with an active differential probe but without the disturbing signal is shown as Figure 5-16. The test procedure is similar with the distortion test by using a pair of SMA cables.

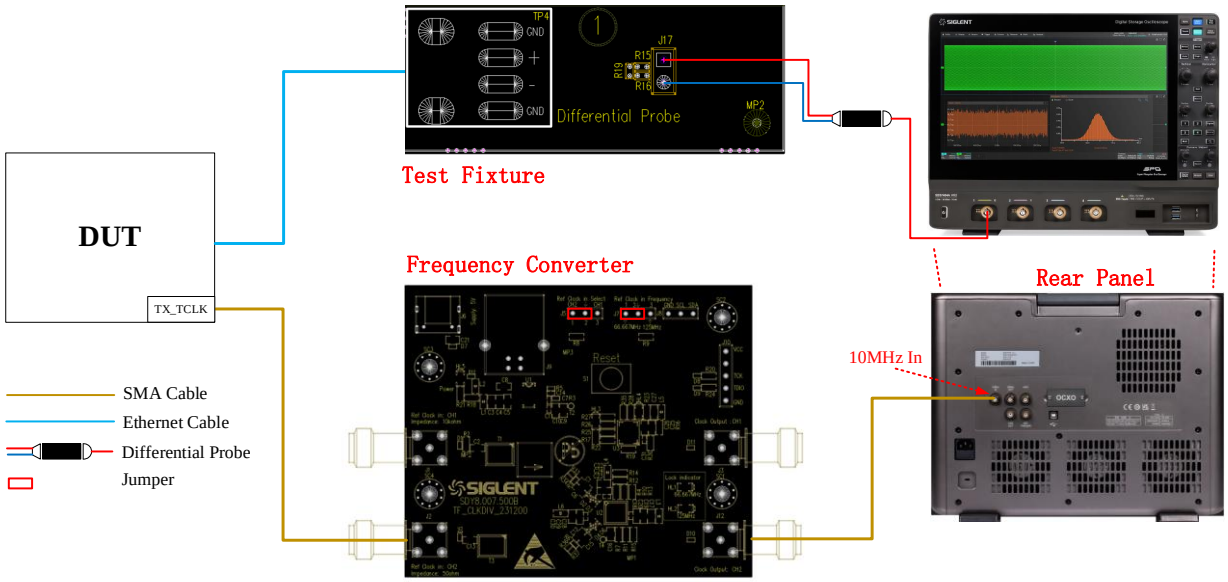


Figure 5-16 Environment setup for transmitter distortion test by using a differential probe (without disturbing signal)

5.4.2 Test procedure

(1) Configure the DUT to output test mode 4 signal.

(2) Select **IEEE** or **OPEN Alliance** specification for the compliance test in **Setup** tab.

(3) Select the **Transmitter Distortion** in the **Test Select** tab.

(4) Set the probe type (differential probe or single-ended input), source channel, with or without disturbing signal in the **Configure** tab.

(5) Check the correctness of the test environment setup in the **Connect** tab.

(6) Click **Run Test** .

(7) If the system is not physically configured to perform this test, the application will return to the **Connect** step to prompt you to change the physical configuration. When you have completed these instructions, click **Run Test** button to resume the test run.

(8) During the test, the Oscilloscope will automatically verify whether the correct test signal is present on the configured DUT “Source” channel, if effective signal is detected, the Oscilloscope will configure the correct trigger level to capture the signal. After finishing the test, the Oscilloscope will output the test result.

5.4.3 Algorithm

The transmitter distortion test is according to the section 96.5.4.2 of IEEE Std 802.3bw specification, and the section OABR_PMA_TX_08 of TC8 ECU specification from OPEN Alliance.

The specifications specify that the Oscilloscope and Arbitrary Waveform Generator are synchronized by the TX_TCLK clock of the DUT. the peak distortion is determined by sampling the differential signal output with the symbol rate clock at an arbitrary phase and processing a block of any 2047 consecutive samples with MATLAB code provided in IEEE Std 802.3bw. The peak distortion values shall be less than 15 mV.

Alternatively, you can run transmitter distortion test without disturbing signal, but the test result is only for informative purpose and it cannot be used to determine the compliance.

5.4.4 Test Result Reference

The transmitter distortion test result is shown in Figure 5-17.

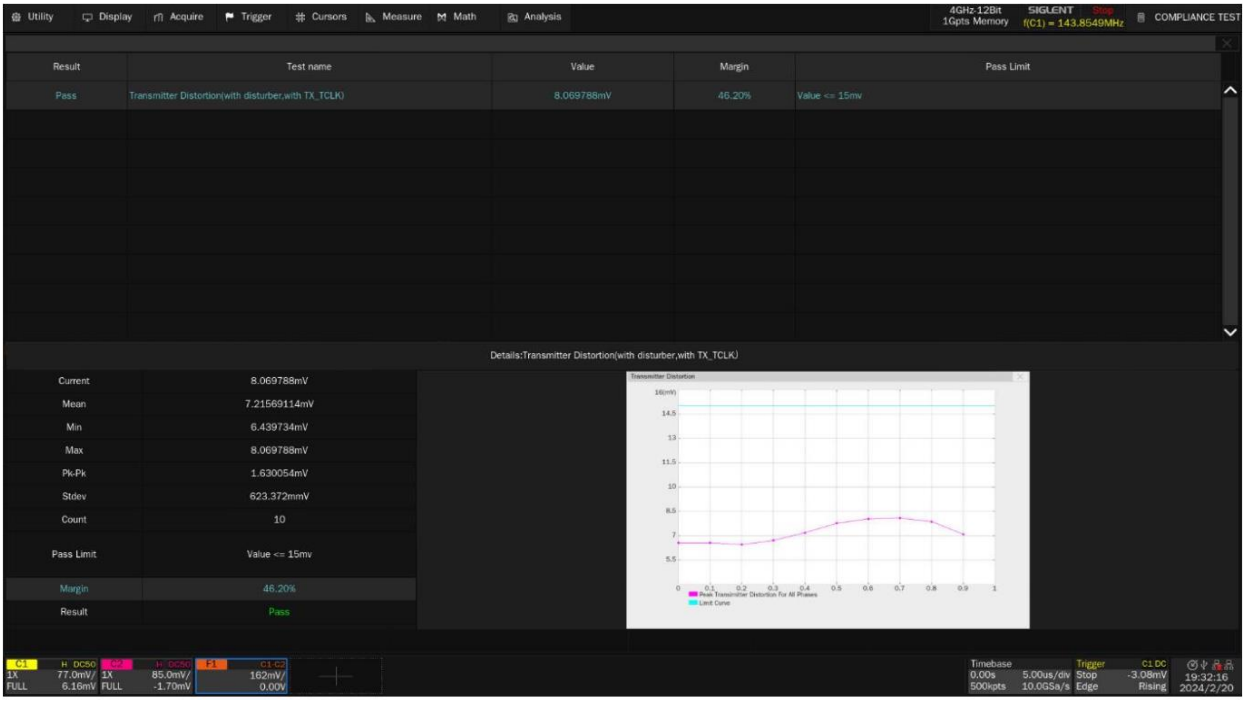


Figure 5-17 Transmitter distortion test result

The details of the test waveform for transmitter distortion test are shown in Figure 5-18.

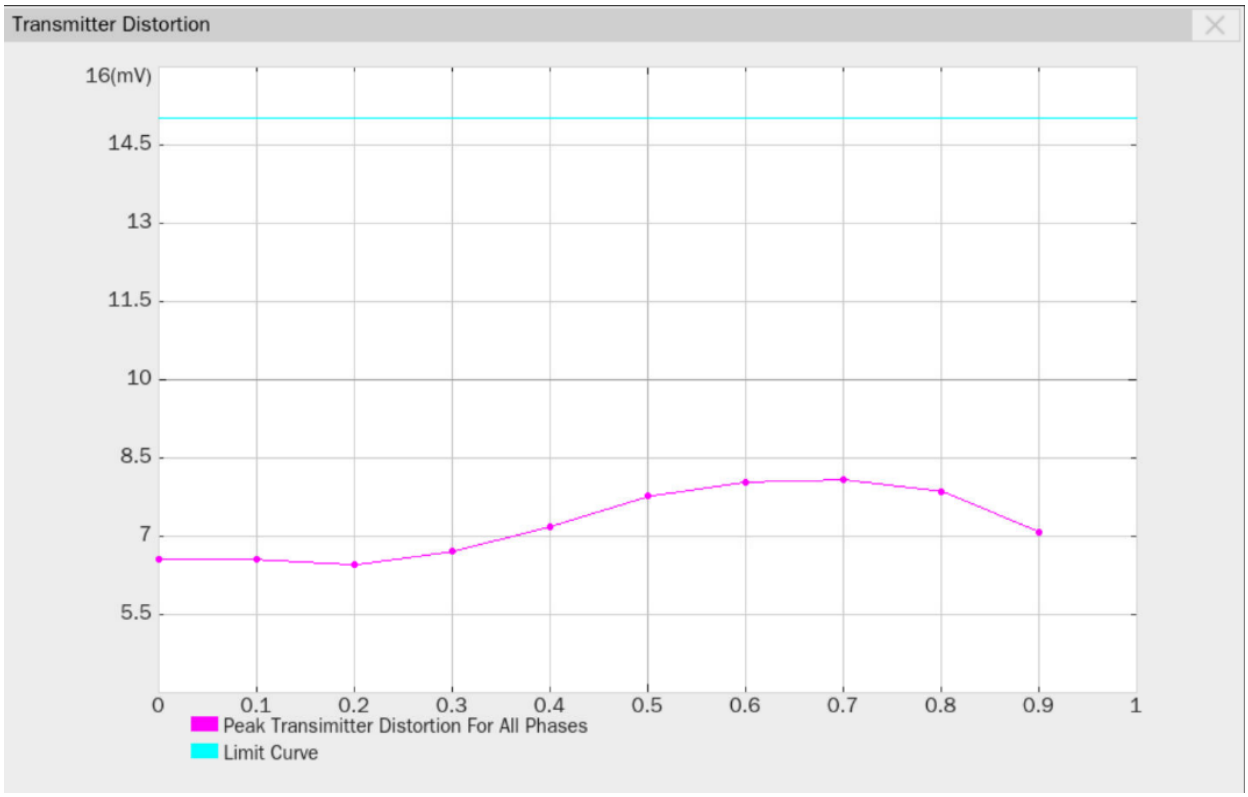


Figure 5-18 Waveform details for transmitter distortion test

5.5 Transmitter Power Spectral Density (PSD) and Peak Differential Output Tests

When test mode 5 is enabled, the PHY is forced to Test Mode 5. In this mode, a pseudo-random sequence of ternary codes {–1, 0, +1}, which are mapped to 3 discrete differential signal levels, is transmitted. Then the user can perform transmitter PSD and peak differential output tests.

Note: There is no peak differential output test requirement in the TC8 ECU specification of Open Alliance, only PSD test is required.

5.5.1 Test Environment and Connectivity

5.5.1.1 Use the Oscilloscope to do PSD and Peak Differential Output Tests

Test environment and connection by using an Oscilloscope for power spectral density and peak differential output tests are the same as <5.1.1 Test Environment and Connectivity> chapter.

The test environment and connection by using a pair of SMA cables is shown in Figure 5-2.

The test environment and connection by using an active differential probe is shown in Figure 5-3.

5.5.1.2 Use a Spectrum Analyzer to do PSD Test

A Spectrum Analyzer can be used to measure the transmitter power spectral density (PSD) to achieve higher measurement accuracy comparing to the Oscilloscope. The connection diagram is shown in Figure 5-19.The measurement procedure is as follows:

(1) Configure the DUT to output the Test Mode 5 signal.

(2) Solder the cable of DUT to TP3 on section ③ of the test fixture.

(3) Use a SMA cable to connect the J12 connector on section ③ of the test fixture to the RF INPUT port on the Spectrum Analyzer.

(4) Use a USB cable to connect the USB Host port on the Oscilloscope to the USB Device port on the Spectrum Analyzer.

(5) In the user interface's **Test Select** tab of the Oscilloscope, click **Transmitter Power Spectral Density**. In the **Configure** tab, click **Transmitter Power Spectral Density** -> **Spectrum Analyzer** -> **Connect Test**, the Oscilloscope will detect the Spectrum Analyzer connection status, if the Spectrum Analyzer is detected, then the Model Name of Spectrum Analyzer will appear, and the Oscilloscope will automatically carry out the Spectrum Analyzer setting (automatically setting only supports Siglent's model). The following is a list of Spectrum Analyzer setup:

- Measurement Unit: dBm;
- Frequency range: 1MHz to 200MHz;
- RBW: 10kHz;
- VBW: 30kHz;

- Detector: RMS Average;
- Frequency Sweep time: 60s.

(6) On the Oscilloscope Click **Run Test** , and click **Run Test** when the pop-up window appears. The Oscilloscope will automatically acquire the power spectral density data tested by the Spectrum Analyzer and plots the curve, after that the Oscilloscope will output the test result.

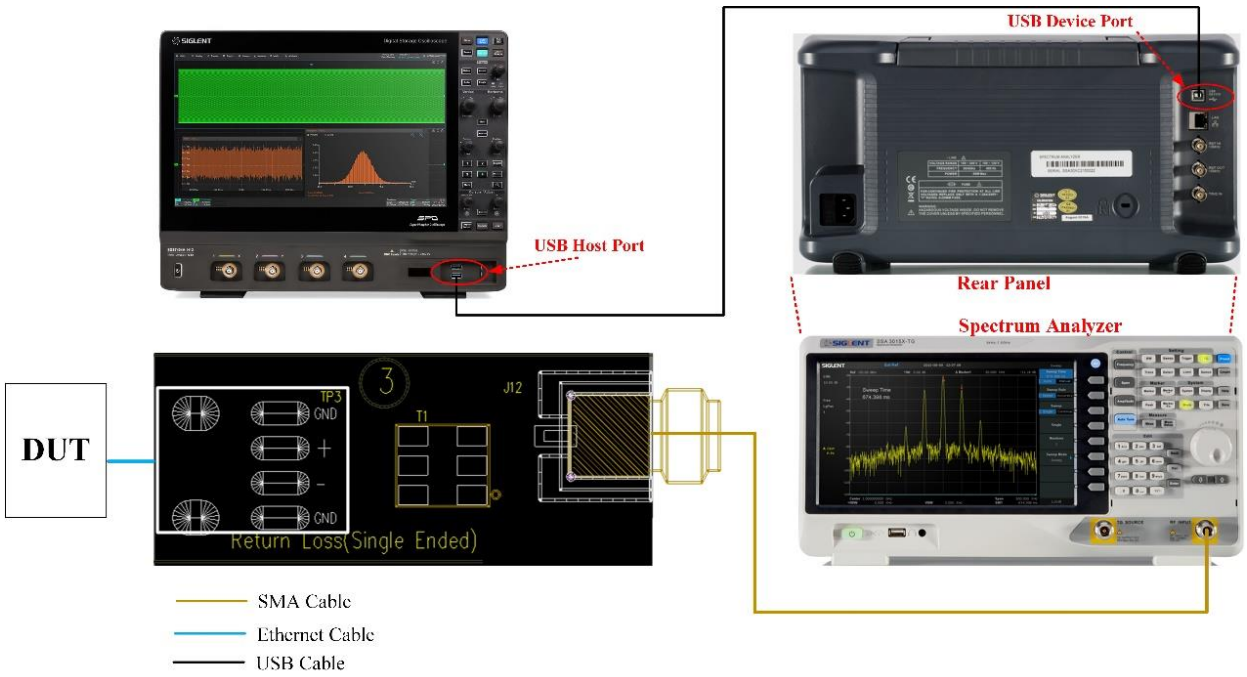


Figure 5-19 Test environment and connection for PSD test by using a Spectrum Analyzer

5.5.2 Test procedure

(1) Configure the DUT to output test mode 5 signal.

(2) Select **IEEE** or **OPEN Alliance** specification for the compliance test in **Setup** tab.

(3) Select the **Transmitter Power Spectral Density and Peak Differential Output** In the **Test Select** tab.

If you select OPEN Alliance specification, only PSD will be tested.

(4) Set the probe type (differential probe or single-ended input), source channel, average number, and whether to use Spectrum Analyzers to do the PSD test in the **Configure** tab.

(5) Check the correctness of the test environment setup in the **Connect** tab.

(6) Click **Run Test** .

(7) If the system is not physically configured to perform this test, the application will return to the **Connect** step to prompt you to change the physical configuration. When you have completed these instructions, click **Run Test** button to resume the test run.

(8) During the test, the Oscilloscope will automatically verify whether the correct test signal is present on the configured DUT “Source” channel, if effective signal is detected, the Oscilloscope will configure the correct trigger level to capture the signal. After finishing the tests, the Oscilloscope

will output the test results.

If you choose to use the Spectrum Analyzers to measure the transmitter power spectral density, the Oscilloscope will control the Spectrum analyzers to perform the measurements and plot the curve according to the Spectrum analyzer's measurement then output the test results.

5.5.3 Algorithm

(1) Transmitter Power spectral density (PSD)

Transmitter Power spectral density (PSD) is specified according to the section 96.5.4.4 of IEEE Std 802.3bw specification, and the section OABR_PMA_TX_04 of TC8 ECU specification from OPEN Alliance.

When DUT outputs Test Mode 5 signal, the transmitter's Power Spectral Density (PSD) shall be between the upper and lower bounds specified in the Figure 5-20.

$$\text{Upper PSD}(f) = \begin{cases} -63.3 - 1.5 \times \frac{f-1}{19} \text{ dBm/Hz} & \text{for } 1 \text{ MHz} \le f < 20 \text{ MHz} \\ -64.8 - 3.7 \times \frac{f-20}{20} \text{ dBm/Hz} & \text{for } 20 \text{ MHz} \le f < 40 \text{ MHz} \\ -68.5 - 8.0 \times \frac{f-40}{17} \text{ dBm/Hz} & \text{for } 40 \text{ MHz} \le f < 57 \text{ MHz} \\ -76.5 \text{ dBm/Hz} & \text{for } 57 \text{ MHz} \le f \le 200 \text{ MHz} \end{cases} \quad (96\text{–}4)$$

$$\text{Lower PSD}(f) = \begin{cases} -70.9 - 4.9 \times \frac{f-1}{19} \text{ dBm/Hz} & \text{for } 1 \text{ MHz} \le f < 20 \text{ MHz} \\ -75.8 - 13.4 \times \frac{f-20}{20} \text{ dBm/Hz} & \text{for } 20 \text{ MHz} \le f < 40 \text{ MHz} \end{cases} \quad (96\text{–}5)$$

where

Upper PSD(f) is the upper limit of the PSD of the transmitted signal frequency f
Lower PSD(f) is the lower limit of the PSD of the transmitted signal frequency f
f is the frequency in MHz

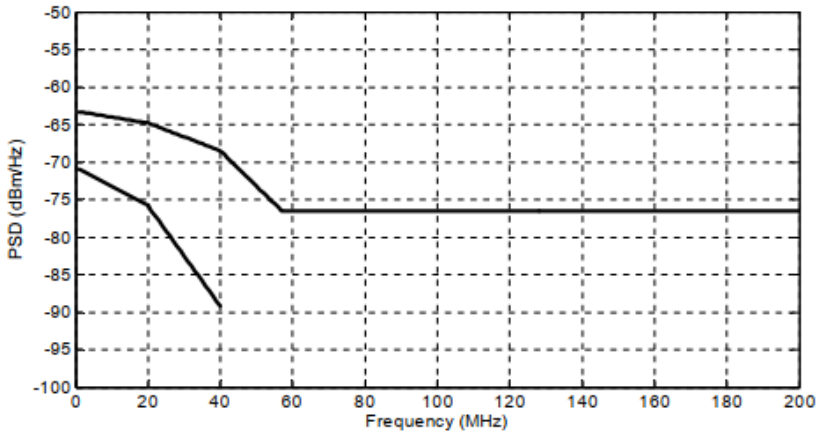


Figure 96–25—PSD upper and lower limits

Figure 5-20 PSD upper and lower limits

(2) Peak differential output

The section 96.5.6 of IEEE Std 802.3bw specification specifies that DUT outputs Test Mode 5 signal, when measured with 100 Ω termination, the transmit differential signal at MDI shall be less than 2.2 Volt peak-to-peak.

5.5.4 Test Results Reference

The test results for the transmitter power spectral density and peak differential output are shown in Figure 5-21, and the waveform details for the transmitter power spectral density is shown in Figure 5-22, the details for peak differential output is shown in Figure 5-23.

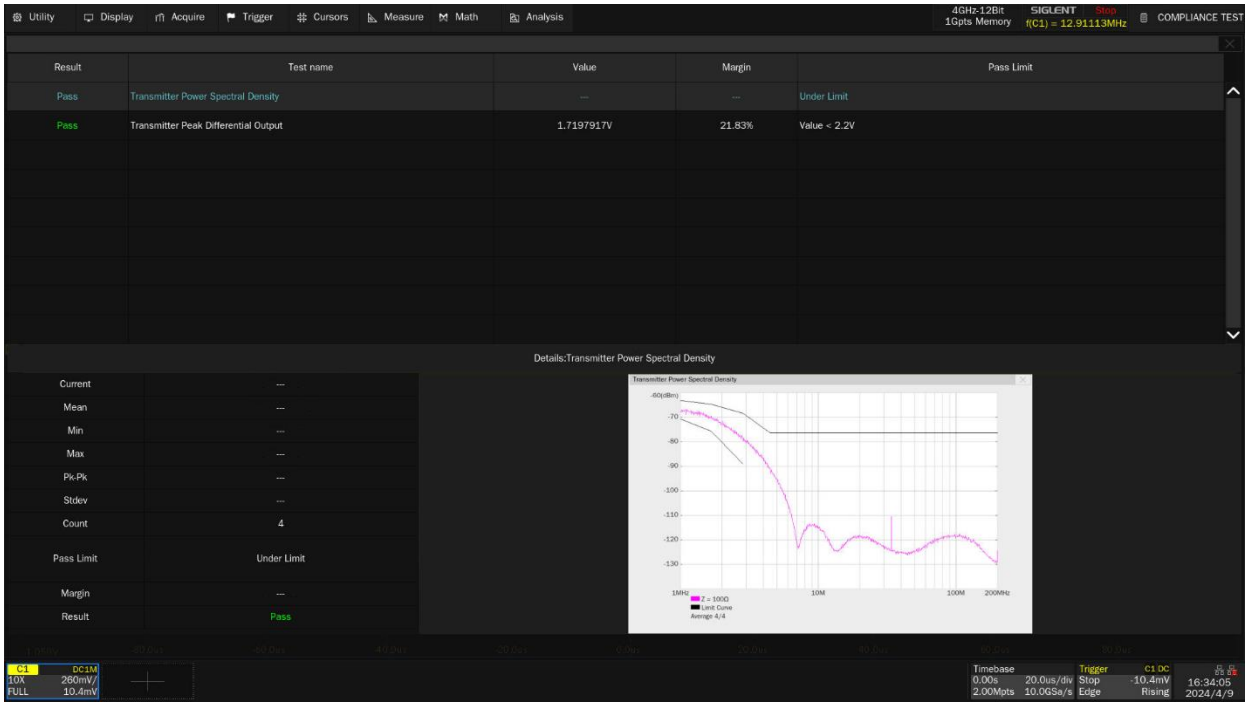


Figure 5-21 PSD and peak differential output test results

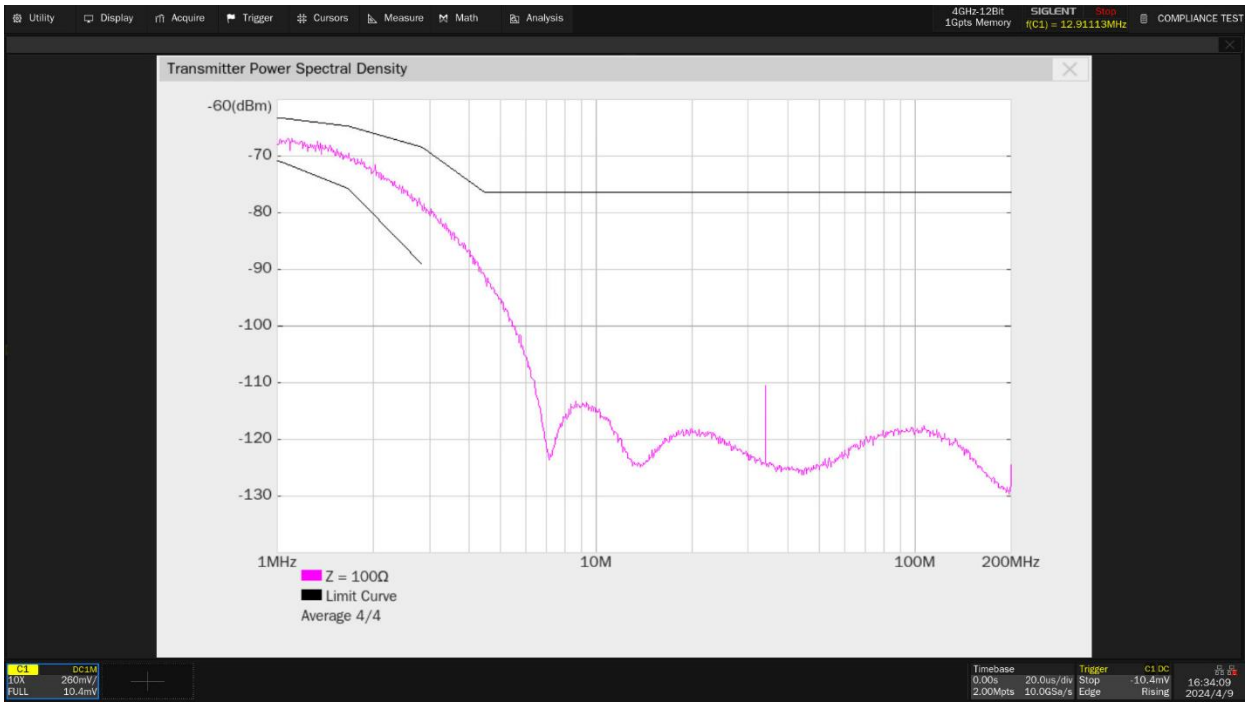


Figure 5-22 Details of transmitted power spectral density waveform

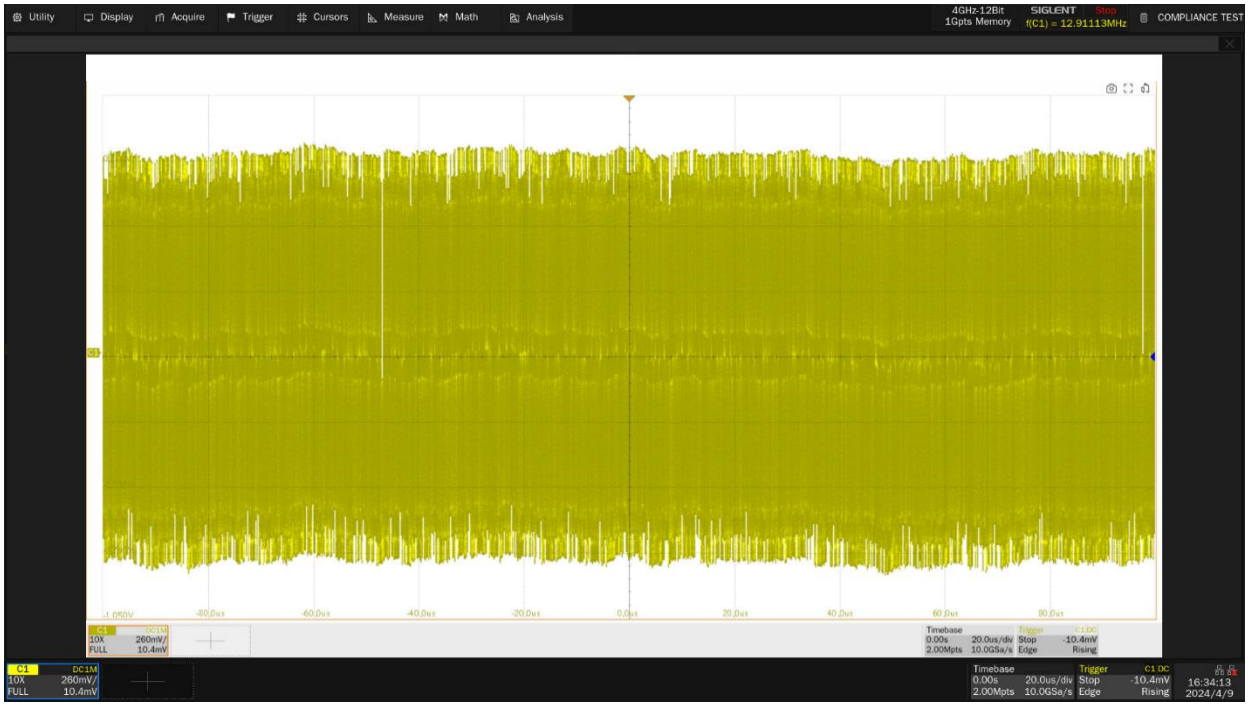


Figure 5-23 Details of peak differential output test result

5.6 MDI Return Loss Tests

The section 96.8.2.1 of IEEE Std 802.3bw specification, and the section OABR_PMA_TX_05 of TC8 ECU specification from OPEN Alliance specify that when doing the MDI return loss test, the DUT must be configured in Slave mode and not transmit any test symbols, the MDI return loss shall be within the specification.

5.6.1 Test Environment and Connectivity

The VNA needs to be calibrated before the running the MDI return loss test.

5.6.1.1 VNA Calibration

Steps for VNA calibration is performed as follows:

(1) Select **IEEE** or **OPEN Alliance** specification for the compliance test in **Setup** tab.

(2) Use a USB cable to connect the USB Host port on the Oscilloscope to the USB Device port on the VNA.

(3) Use two SMA cables with equal length to connect two Ports of the VNA, and to the Calibration Kit.

In the user interface's **Test Select** tab of the Oscilloscope, click **MDI Return Loss**. In the **Configure** tab, click **Connect Test**, the Oscilloscope will detect the VNA connection status, if the VNA is detected, then the Model Name of VNA will appear, and the Oscilloscope will automatically carry out the VNA setting (automatically setting only supports Siglent's model). The following is a list of VNA setup:

- Measurement: Return Loss (Sdd11)
- Start frequency: 1MHz (IEEE specification), 0.3MHz (Open Alliance specification)
- Stop frequency: 66MHz (IEEE specification), 1GHz (Open Alliance specification)
- Sweep type: Logarithmic
- Sweep points: 1601
- Output power: -10dBm(min), 0dBm (Recommended)
- IF Bandwidth: 100Hz
- Logic port impedance differential mode: 100Ω
- Logic port impedance common mode: 25Ω
- Smooth function is deactivated

(4) In the **Configure** -> **MDI Return Loss**, set the measurement type to **Balanced Measure**.

(5) Set the calibration parameters of VNA for Open, Load, Short and Through calibration.

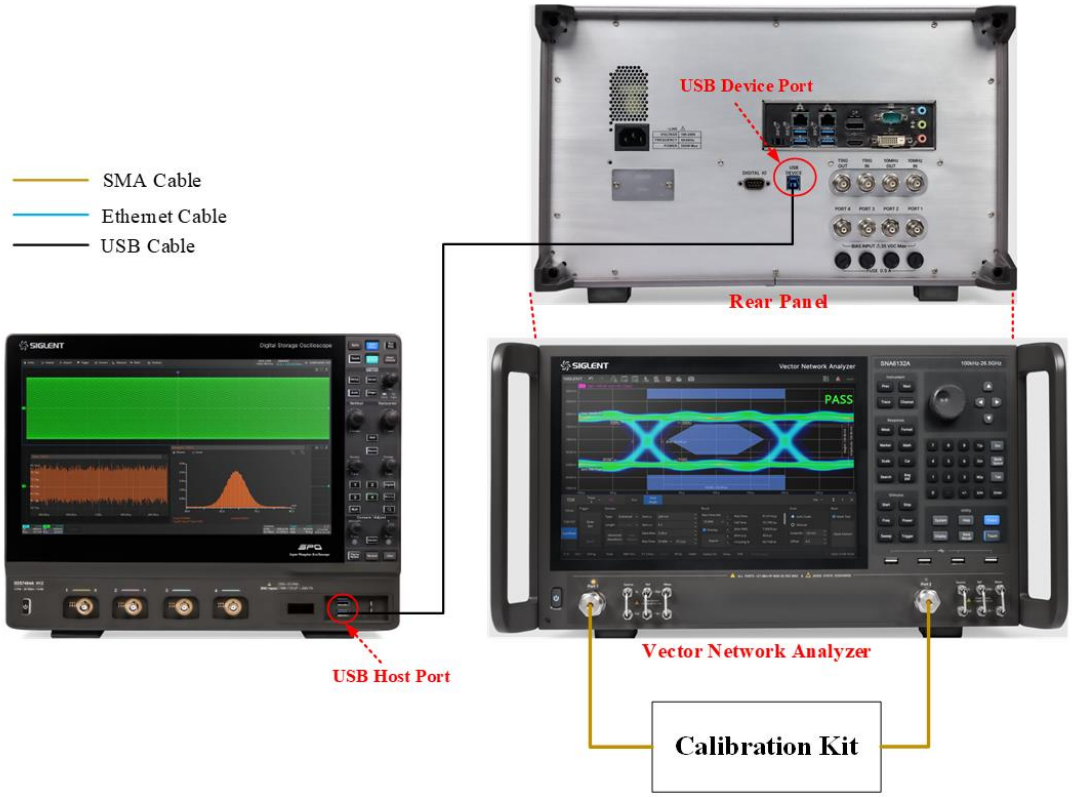


Figure 5-24 Calibration environment for return loss by using Balanced Measure method

The user can also use a single port on VNA to perform the MDI return loss test, In the **Configure** -> **MDI Return Loss**, set the measurement type to **S-params**. The user needs to make an 50Ω to 100Ω transition adapter. Before performing MDI return loss test, the VNA needs to be calibrated, the calibration environment is shown in Figure 5-25.

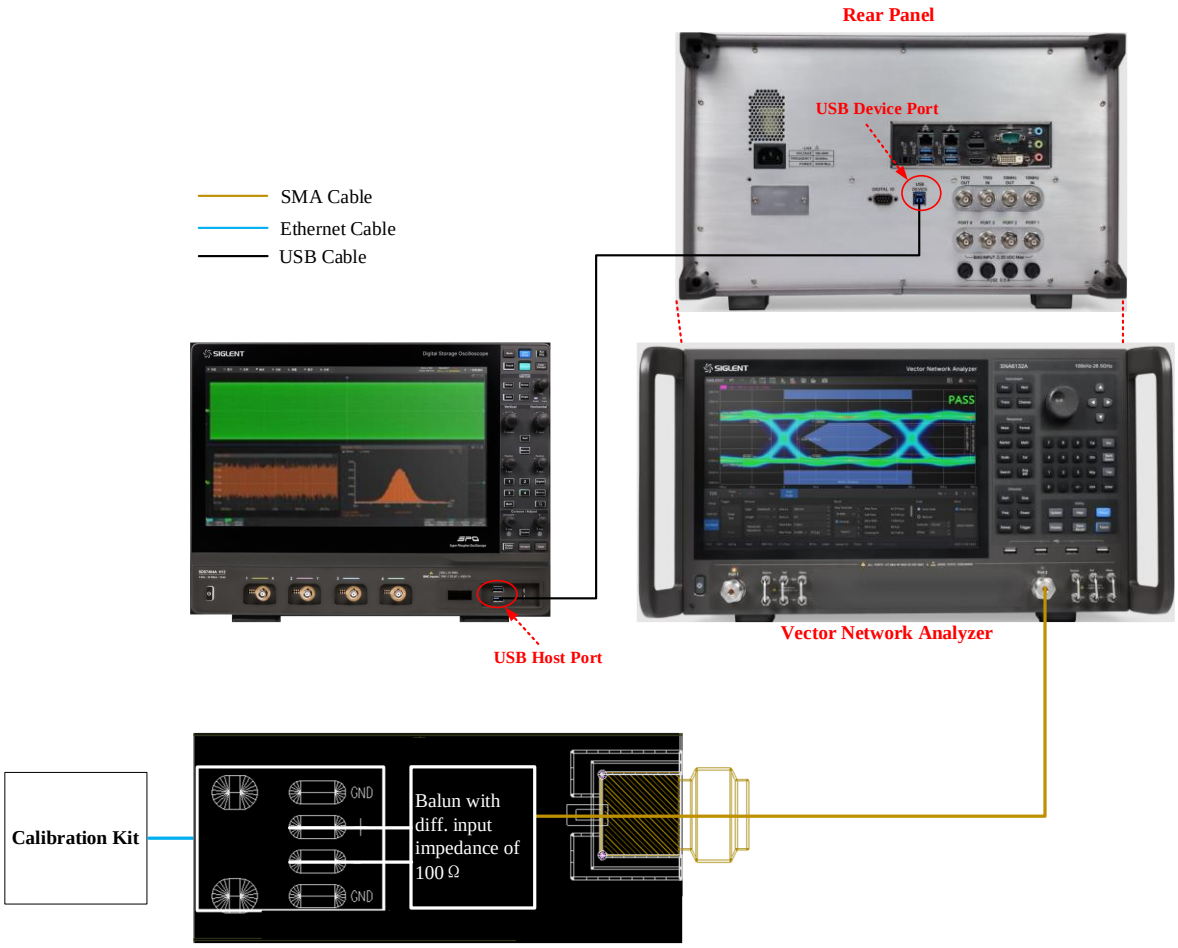


Figure 5-25 Calibration environment for return loss by using S-params method

5.6.1.2 Test Environment for MDI Return Loss Test

The test environment for the MDI return loss by using balanced measurement method is shown in Figure 5-26. The test procedure is as follows:

(1) The DUT must be set to Slave Mode of operation and not transmitting any test symbols.

(2) Use two SMA cables with equal length to connect the test points J1(+) and J4(-) on section ④ of the test fixture, and to two ports on the VNA which are selected for measurement.

(3) Solder the cable of DUT to TP2 on section ④ of the test fixture.

(4) Use a USB cable to connect the USB Host port on the Oscilloscope to the USB Device port on the VNA.

(5) In the **Configure** -> **MDI Return Loss**, set the measurement type to **Balanced Measure**.

(6) On the Oscilloscope Click **Run Test**, and check the correctness of the test environment setup before click **Run Test** when the pop-up window appears. The Oscilloscope will automatically

acquire the return loss data tested by the VNA and plots the curve, and outputs the test result.

Note: Please ensure the cable from DUT to the TP2 is as short as possible, which will get higher measurement accuracy results.

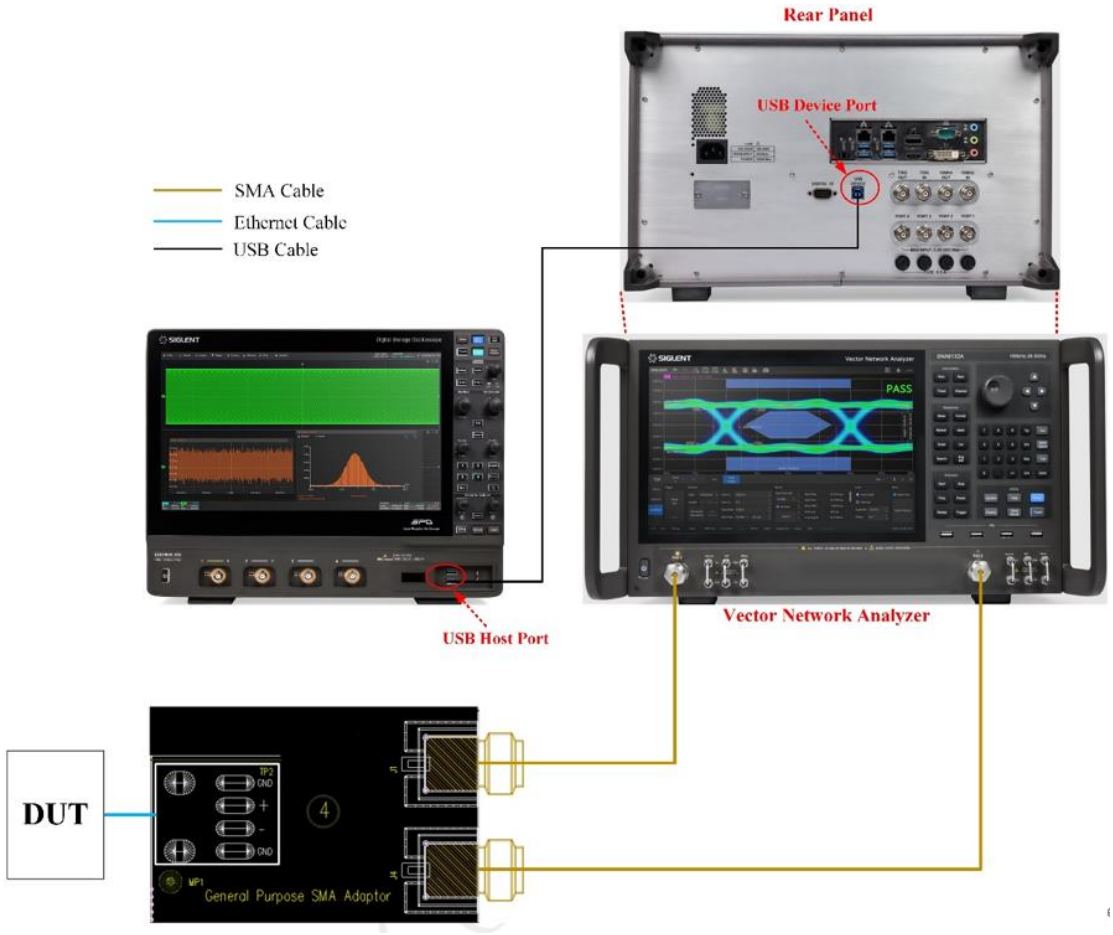


Figure 5-26 Connection for MDI return loss by using balanced measurements

The test environment for the MDI return loss by using S parameter method is shown in Figure 5-27. The test procedure is as follows:

(1) The DUT must be set to Slave Mode of operation and not transmitting any test symbols.

(2) Use one SMA cable to connect to the Adaptor which has the function of conversion the differential 100Ω to 50Ω, and to one port on the VNA which is selected for measurement.

(3) Use a USB cable to connect the USB Host port on the Oscilloscope to the USB Device port on the VNA.

(4) In the **Configure** -> **MDI Return Loss**, set the measurement type to **S-params**.

(5) On the Oscilloscope Click **Run Test**, and check the correctness of the test environment setup before click **Run Test** when the pop-up window appears. The Oscilloscope will automatically acquire the return loss data tested by the VNA and plots the curve, and outputs the test result.

Note: Please ensure the cable from DUT to the Adapter is as short as possible, which will get higher measurement accuracy results.

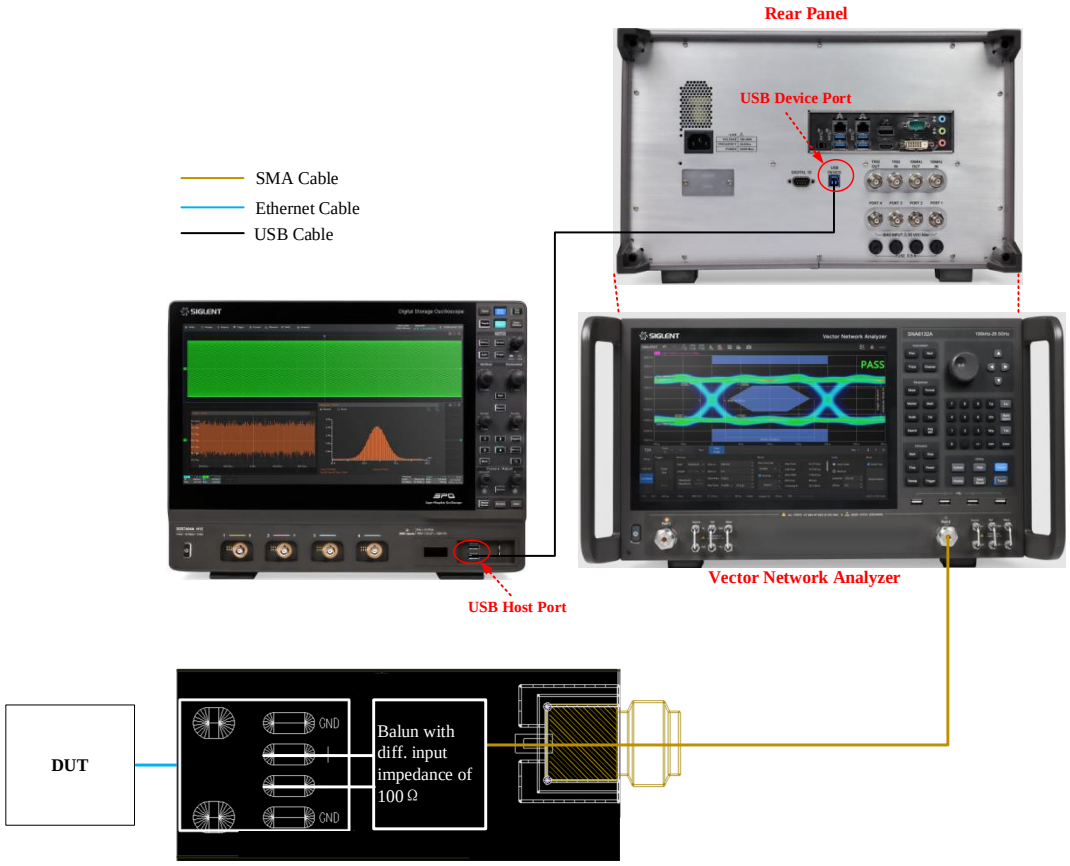


Figure 5-27 Connection for MDI return loss by using S-parameter method

5.6.2 Test procedure

(1) The DUT must be set to Slave Mode and not transmitting any test symbols.

(2) Select **IEEE** or **OPEN Alliance** specification for the compliance test in **Setup** tab.

(3) Select **MDI Return Loss** In the **Test Select** tab.

(4) In the **Configure** tab, click **Connect Test** , the Oscilloscope will detect the VNA connection status, if the VNA is detected, then the Model Name of VNA will appear

(5) in the **Configure** tab, select **Balanced Measure** or **S-params** .

(6) Check the correctness of the test environment setup in the **Connect** tab. The VNA should be finished calibrating before doing the MDI return loss test.

(7) Click **Run Test** .

(8) If the system is not physically configured to perform this test, the application will return to the **Connect** step to prompt you to change the physical configuration. When you have completed

these instructions, click **Run Test** button to resume the test run.

(9) During the test, the Oscilloscope will automatically control the VNA to perform the MDI return loss measurements and plot the curve according to the VNA's measurement then output the test result.

5.6.3 Algorithm

Section 96.8.2.1 of the IEEE Std 802.3bw specification and Section OABR_PMA_TX_05 of Open Alliance TC8 ECU specification both specify that the MDI return loss (RL) shall meet or better than the following limits for all frequencies from 1 MHz to 66 MHz (with 100 Ω impedance termination) at all times when the PHY is transmitting data or control symbols.

- MDI return loss should be smaller than -20dB at the frequency range of 1MHz to 30MHz.
- MDI return loss should be smaller than -（20-20×log10(f/30)）at the frequency range of 30MHz to 66MHz.

Note: For the Open Alliance TC8 ECU specification, the frequency range of MDI return loss test is from 300kHz to 1GHz, while frequency range of the limit is only specified from 1 MHz to 66 MHz.

5.6.4 Test Result Reference

According to IEEE specification, the test result of the MDI return loss is shown in Figure 5-28. The waveform details are shown in Figure 5-29.

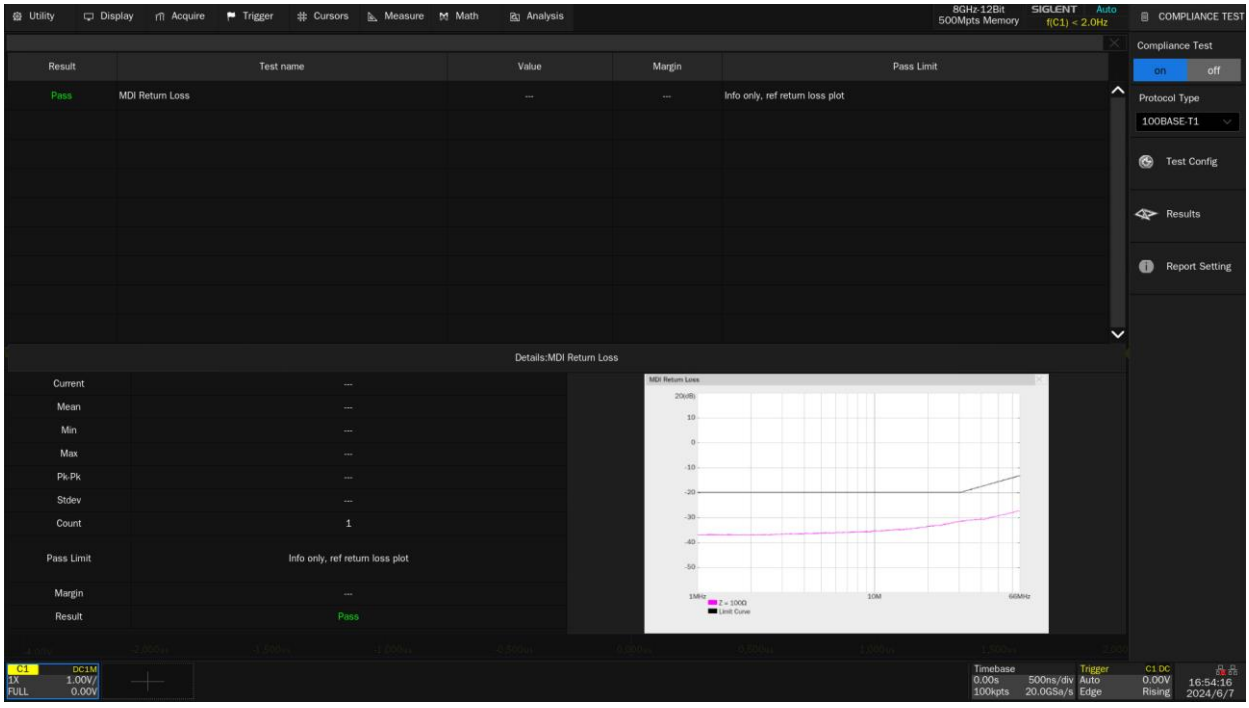


Figure 5-28 Test result of the MDI return loss according to IEEE specification

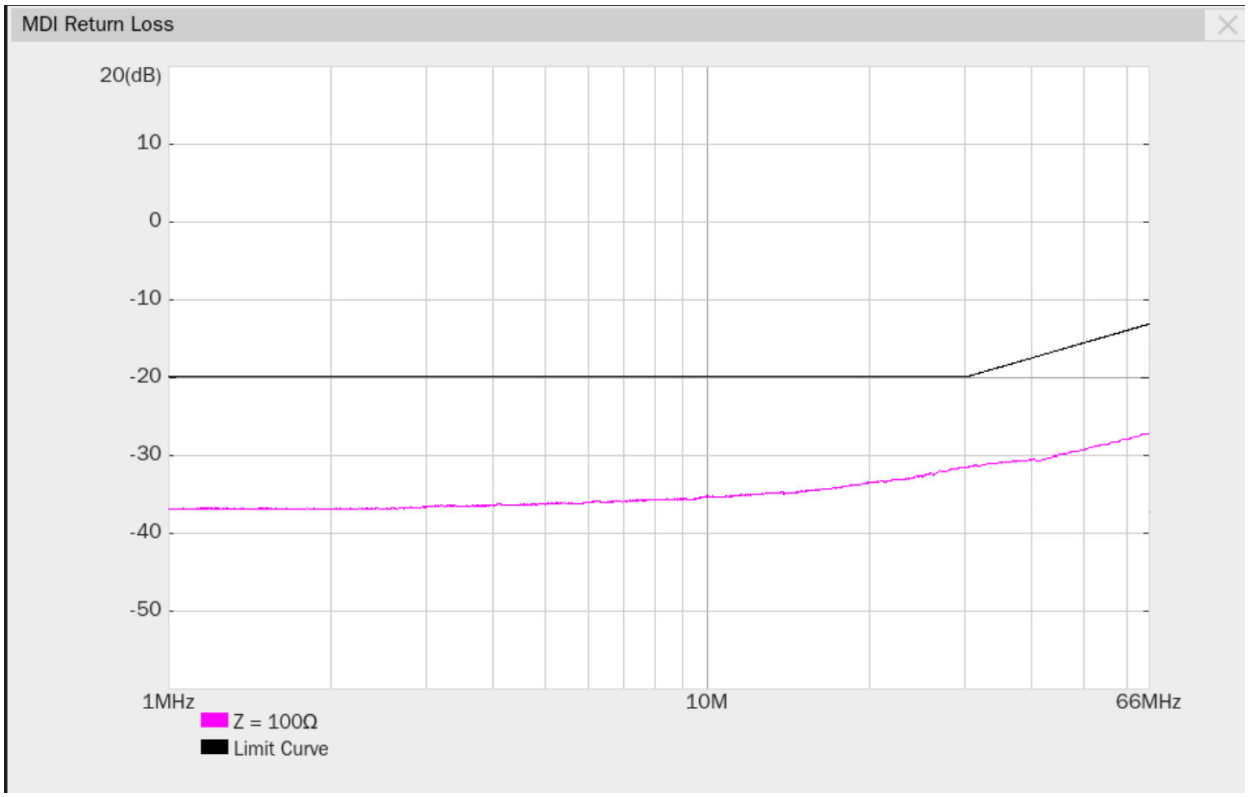


Figure 5-29 Waveform details of the MDI return loss according to IEEE specification

According to Open Alliance specification, the test result of the MDI return loss is shown in Figure 5-30. The waveform details are shown in Figure 5-31.

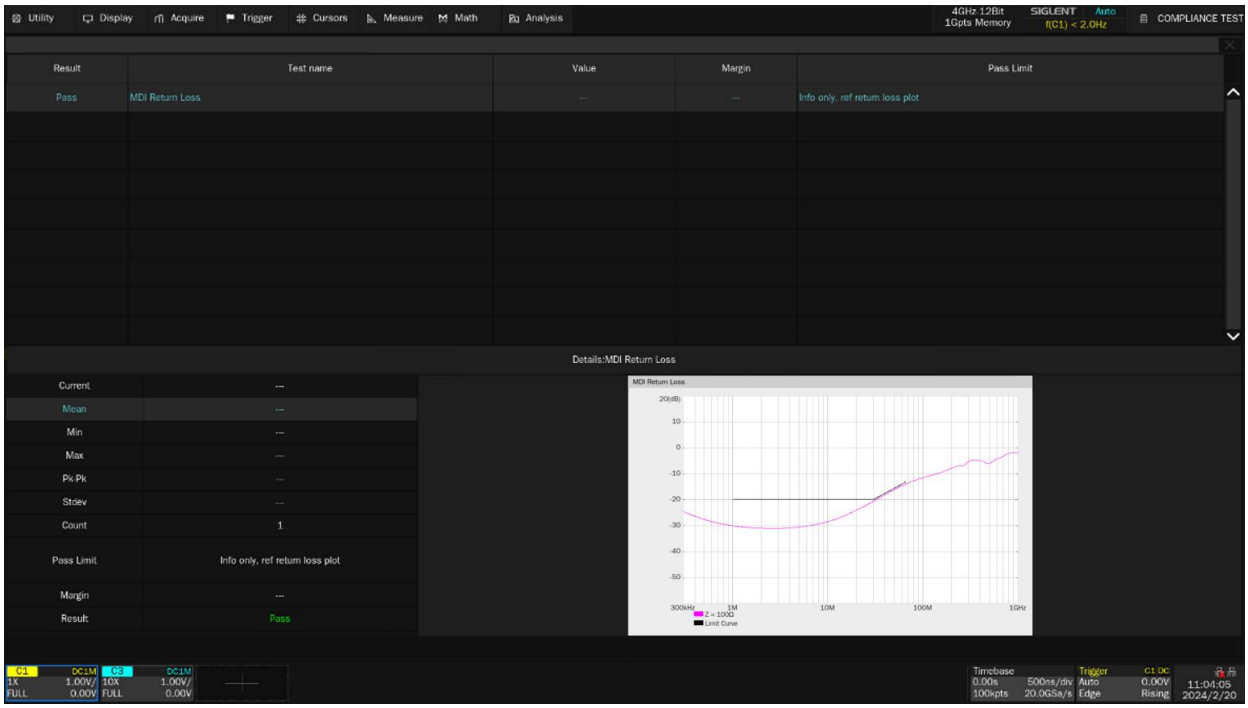


Figure 5-30 Test result of the MDI return loss according to Open Alliance specification

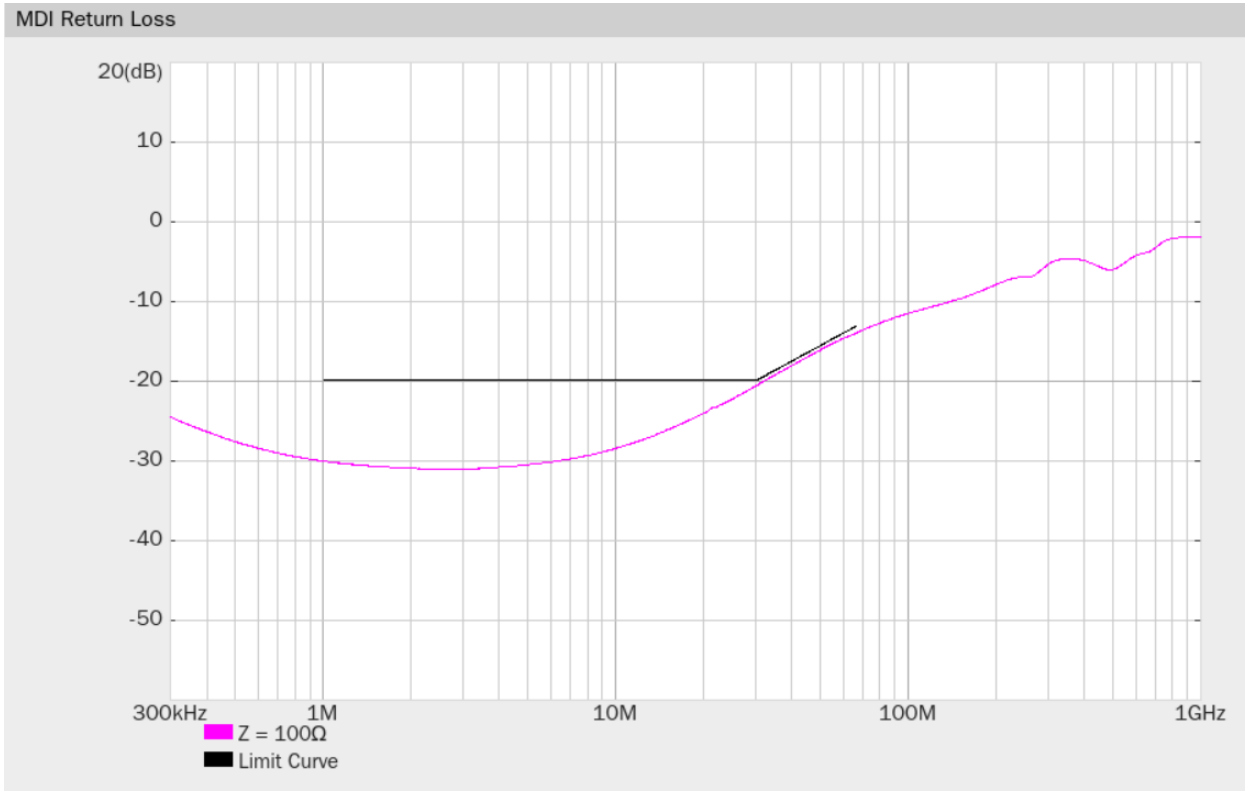


Figure 5-31 Waveform details of the MDI return loss according to Open Alliance specification

5.7 MDI Mode Conversion Loss Tests

Section 96.8.2.2 of the IEEE Std 802.3bw specification and the section "OABR_PMA_TX_06: Check MDI Mode Conversion" of the TC8 OPEN Alliance Automotive Ethernet ECU Test Specification specify that the MDI mode conversion loss (Sdc11) of the transmitter (with 100 Ω impedance termination) shall be within the limits at all times when the PHY is transmitting data or control symbols. When doing the MDI mode conversion loss test, the DUT must be configured in Slave mode and not transmit any test symbols.

5.7.1 Test Environment and Connectivity

The VNA needs to be calibrated before running the MDI mode conversion loss test.

5.7.1.1 VNA Calibration

The VNA calibration can be used the SOLT or SOLR calibration method. But the TRL can achieve very high precision because the two-port TRL calibration method does not need to know the index parameters of the calibration kit, and all the error items in the error model of the test device can be figured out through three simple connection methods. TRL calibration scheme will use the THRU straight through calibration element, reflection calibration kit (Open or Short), and a small section of

transmission line. Through TRL calibration method, the measurement error due to the test fixture can be minimized.

Note: If the LINE standard of appropriate length or loss cannot be fabricated, a MATCH standard maybe used instead of the LINE. The MATCH standard may be defined as an infinite length transmission line OR as a 1-port low reflect termination, such as a load.

Calibration environment and connection for VNA is shown in Figure 5-32. Steps for VNA calibration is performed as follows:

(1) Select **IEEE** or **OPEN Alliance** specification for the compliance test in **Setup** tab.

(2) Use a USB cable to connect the USB Host port on the Oscilloscope to the USB Device port on the VNA.

(3) Use two SMA cables with equal length to connect two Ports of the VNA, and to the Calibration Kit.

(4) In the user interface's **Test Select** tab of the Oscilloscope, click **MDI Mode Conversion Loss**. In the **Configure** tab, click **MDI Mode Conversion Loss** -> **Connect Test** , the Oscilloscope will detect the VNA connection status, if the VNA is detected, then the Model Name of VNA will appear, and the Oscilloscope will automatically carry out the VNA setting (automatically setting only supports Siglent's model). The following is a list of VNA setup:

- Measurement: Return Loss（Sdc11）
- Start frequency: 1MHz (IEEE specification), 0.3MHz (Open Alliance specification)
- Stop frequency: 66MHz (IEEE specification), 1GHz (Open Alliance specification)
- Sweep type: Logarithmic
- Sweep points: 1601
- Output power: -10dBm(min), 0dBm (Recommended)
- IF Bandwidth: 100Hz
- Logic port impedance differential mode: 100Ω
- Logic port impedance common mode: 25Ω
- Smooth function is deactivated

(5) Set the calibration parameters of VNA for Open, Load, Short and Through calibration with the SOLT or SOLR calibration method, or Reflect, Through, Line calibration with the RTL calibration method.

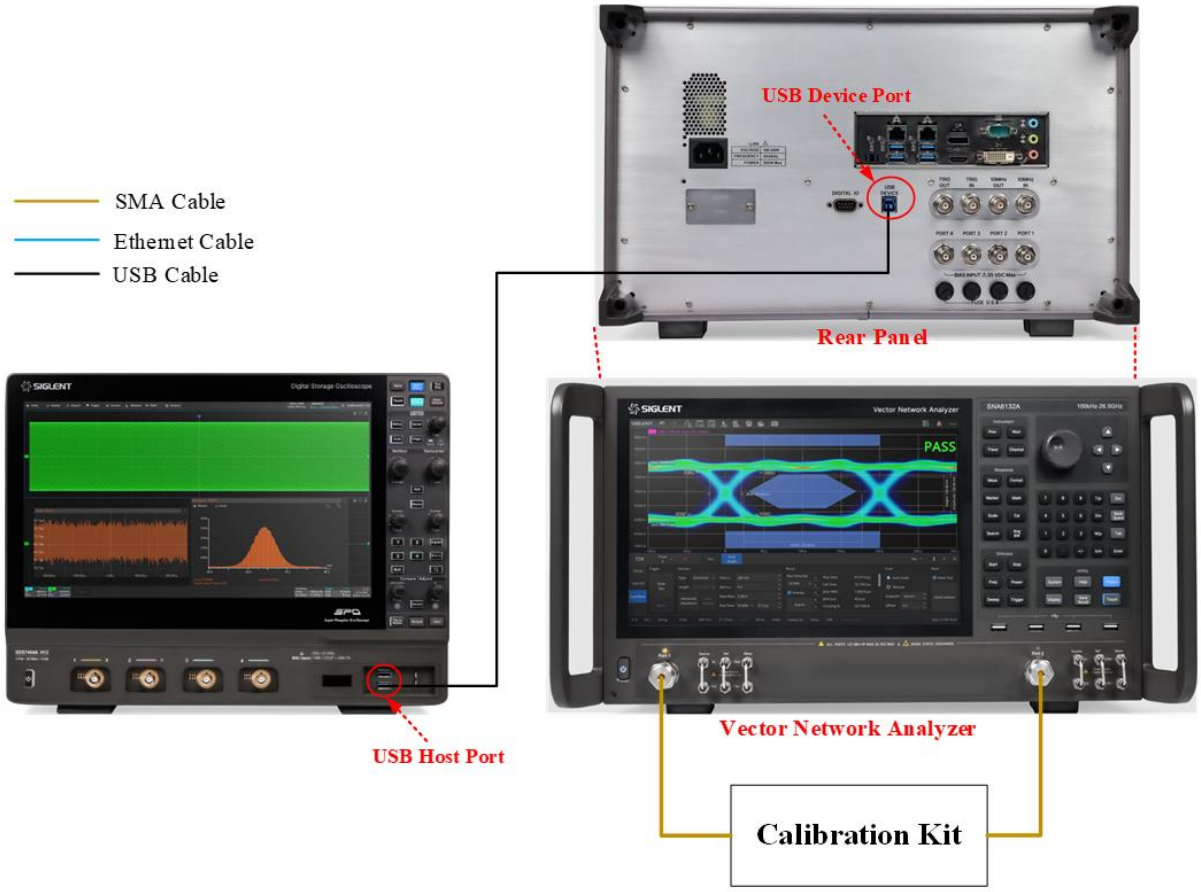


Figure 5-32 Calibration environment for return loss by using Balanced Measure method

5.7.1.2 Test Environment for MDI Mode Conversion Loss Test

Test environment and connection for MDI mode conversion loss test is shown in Figure 5-33. The procedure for measuring MDI mode conversion loss is as follows:

(1) The DUT must be set to Slave Mode of operation and not transmitting any test symbols.

(2) Use two SMA cables with equal length to connect the test points J1(+) and J4(-) on section ④ of the test fixture, and to two ports on the VNA which are selected for measurement.

(3) Solder the cable of DUT to TP2 on section ④ of the test fixture.

(4) Use a USB cable to connect the USB Host port on the Oscilloscope to the USB Device port on the VNA.

(5) On the Oscilloscope Click **Run Test**, and check the correctness of the test environment setup before click **Run Test** when the pop-up window appears. The Oscilloscope will automatically acquire the mode conversion loss data tested by the VNA and plots the curve, and outputs the test result.

Note: Please ensure the cable from DUT to the TP2 is as short as possible, which will get higher measurement accuracy results.

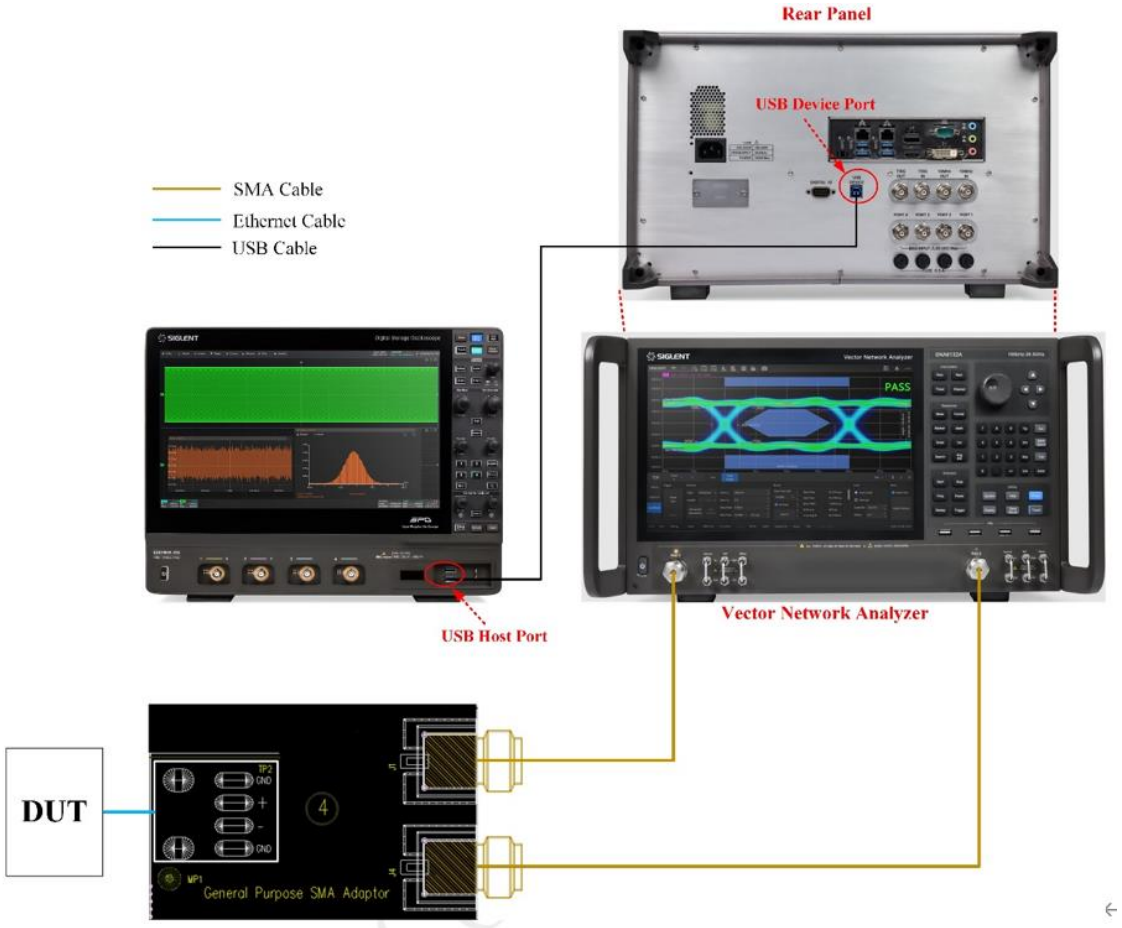


Figure 5-33 Test environment and connection for MDI mode conversion loss test

5.7.2 Test procedure

(1) The DUT must be set to Slave Mode and not transmitting any test symbols.

(2) Select **IEEE** or **OPEN Alliance** specification for the compliance test in **Setup** tab.

(3) Select the **MDI Mode Conversion Loss** In the **Test Select** tab.

(4) In the **Configure** tab, click **Connect Test**, the Oscilloscope will detect the VNA connection status, if the VNA is detected, then the Model Name of VNA will appear

(5) Check the correctness of the test environment setup in the **Connect** tab. The VNA should be finished calibrating before doing the MDI mode conversion loss test.

(6) Click **Run Test** .

(7) If the system is not physically configured to perform this test, the application will return to the **Connect** step to prompt you to change the physical configuration. When you have completed these instructions, click **Run Test** button to resume the test run.

(8) During the test, the Oscilloscope will automatically control the VNA to perform the MDI mode conversion loss measurements and plot the curve according to the VNA's measurement then output the test results.

5.7.3 Algorithm

The MDI mode conversion loss test has two specifications, which are:

(1) IEEE Std 802.3bw-2015 specification

Section 96.8.2.2 of the IEEE Std 802.3bw specification specifies that the Mode conversion LCL (Sdc11) of the PHY measured at MDI shall meet or better than the limit defined as below for all frequencies from 1 MHz to 200 MHz.

- MDI return loss should be smaller than -50dB at frequency range of 1MHz to 33MHz.
- MDI return loss should be smaller than -(50-20×log10(f/33)) at frequency range of 33MHz to 200 MHz.

(2) Open Alliance TC8 ECU specification

The section OABR_PMA_TX_05 of Open Alliance TC8 ECU specification specifies that the Mode conversion LCL (Sdc11) of the PHY measured at MDI shall meet or better than the limit defined as below for all frequencies from 1 MHz to 200 MHz.

- MDI return loss should be smaller than -60dB at frequency range of 1MHz to 22 MHz.
- MDI return loss should be smaller than -(60-20×log10(f/22)) at frequency range of 22 MHz to 100 MHz.
- MDI return loss should be smaller than -(47-30×log10(f/100)) at frequency range of 100 MHz to 200 MHz.

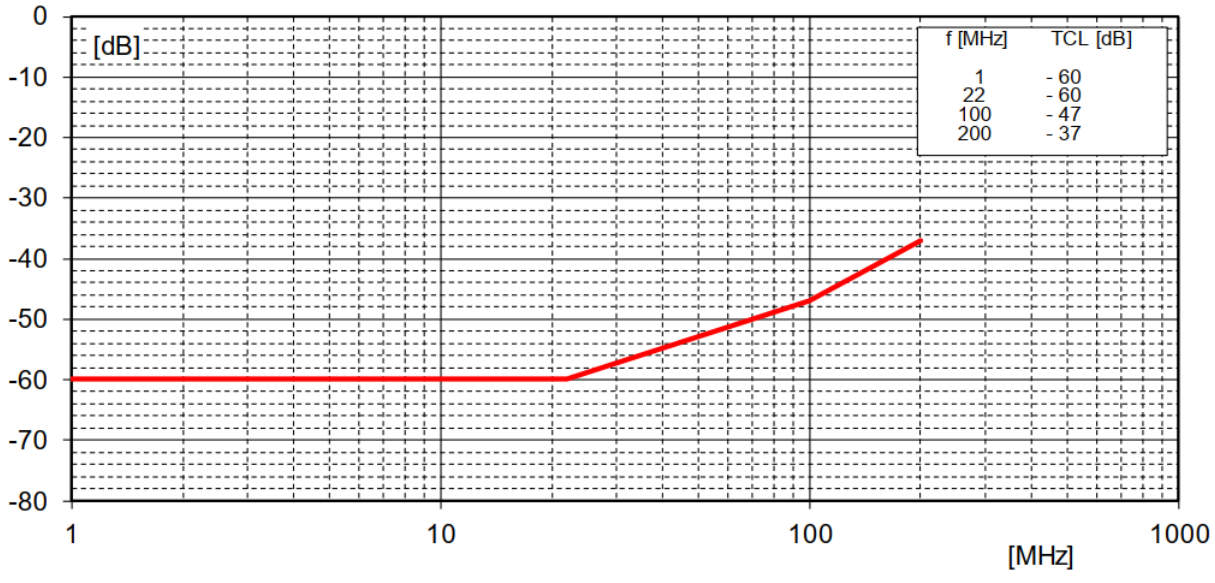


Figure 5-34 MDI mode conversion loss threshold for ECU on TC8 specification

5.7.4 Test Results Reference

The test result of the MDI mode conversion loss with IEEE specification is shown in Figure 5-35. The waveform details are shown in Figure 5-36.

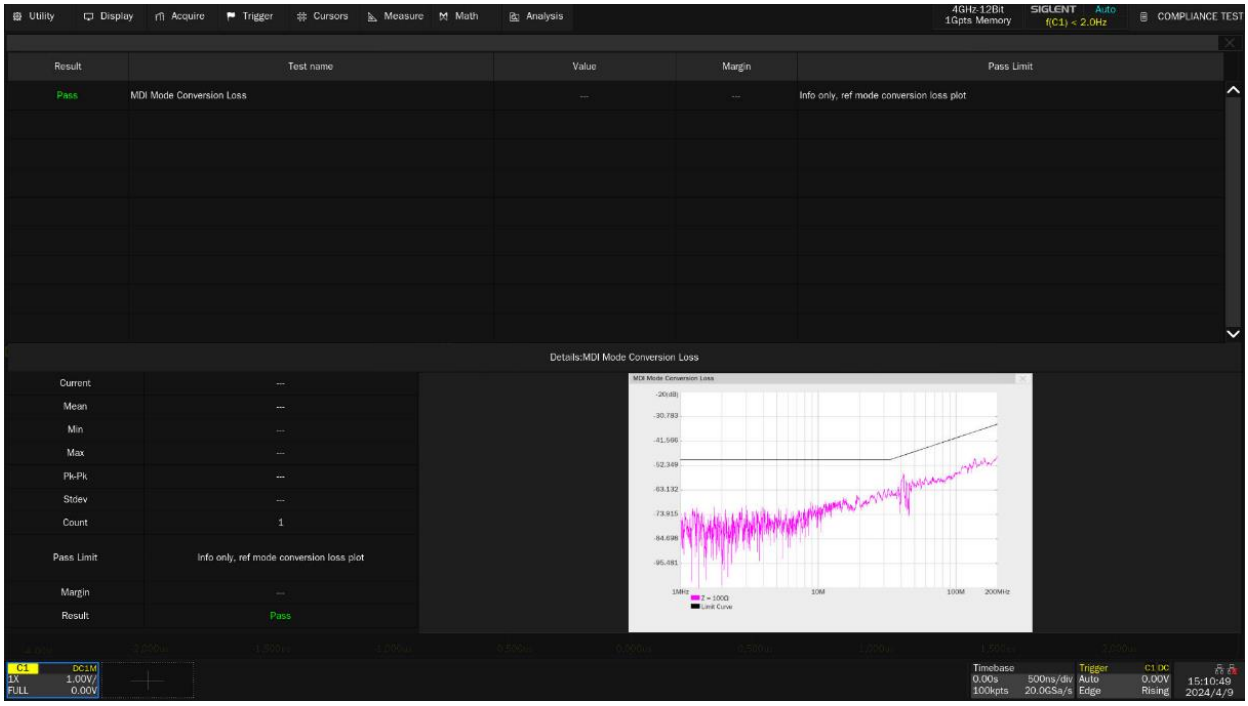


Figure 5-35 Test result of the MDI mode conversion loss with IEEE specification

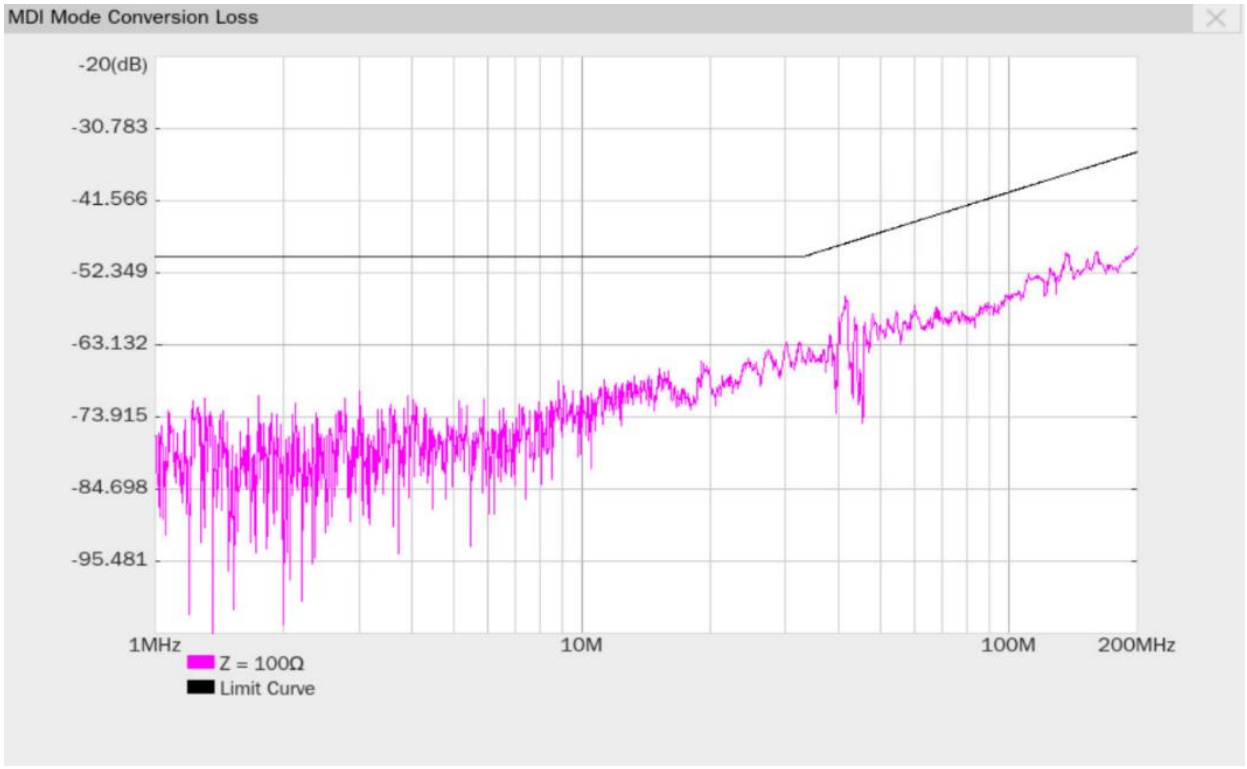


Figure 5-36 Waveform details of the MDI mode conversion loss with IEEE specification

The test result of the MDI mode conversion loss with TC8 ECU specification is shown in Figure 5-37. The waveform details are shown in Figure 5-38.

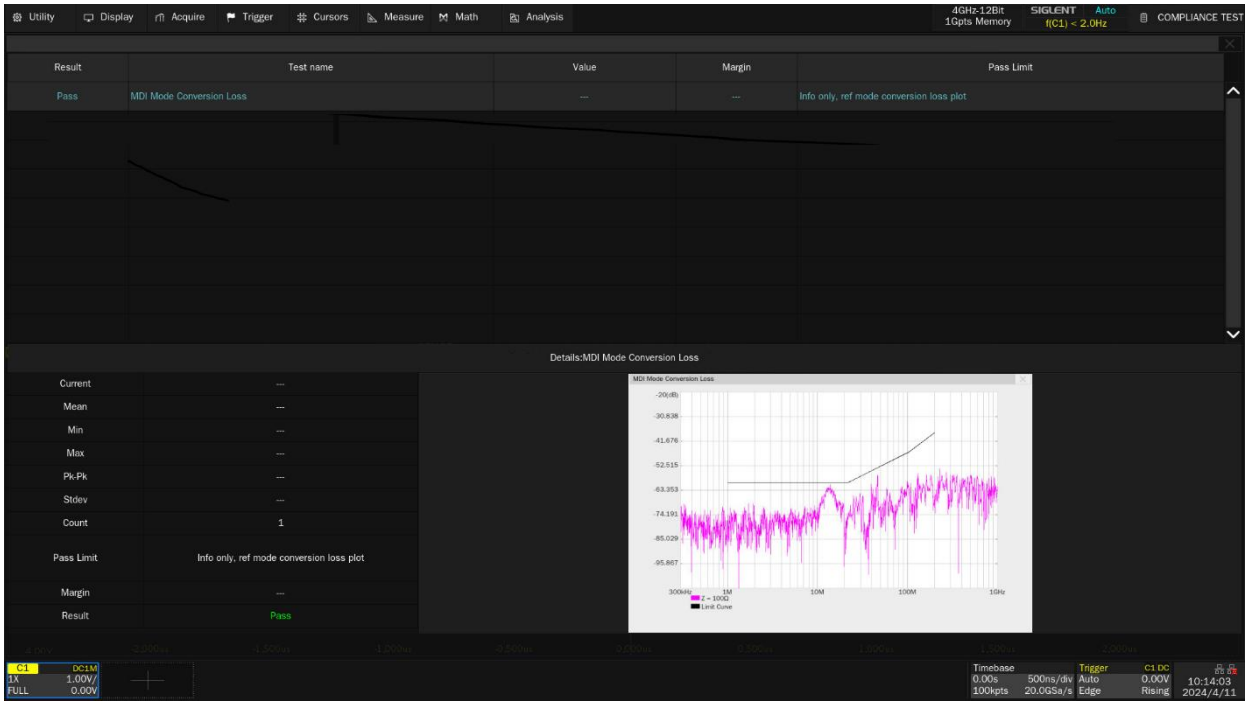


Figure 5-37 Test result of the MDI mode conversion loss with TC8 ECU specification

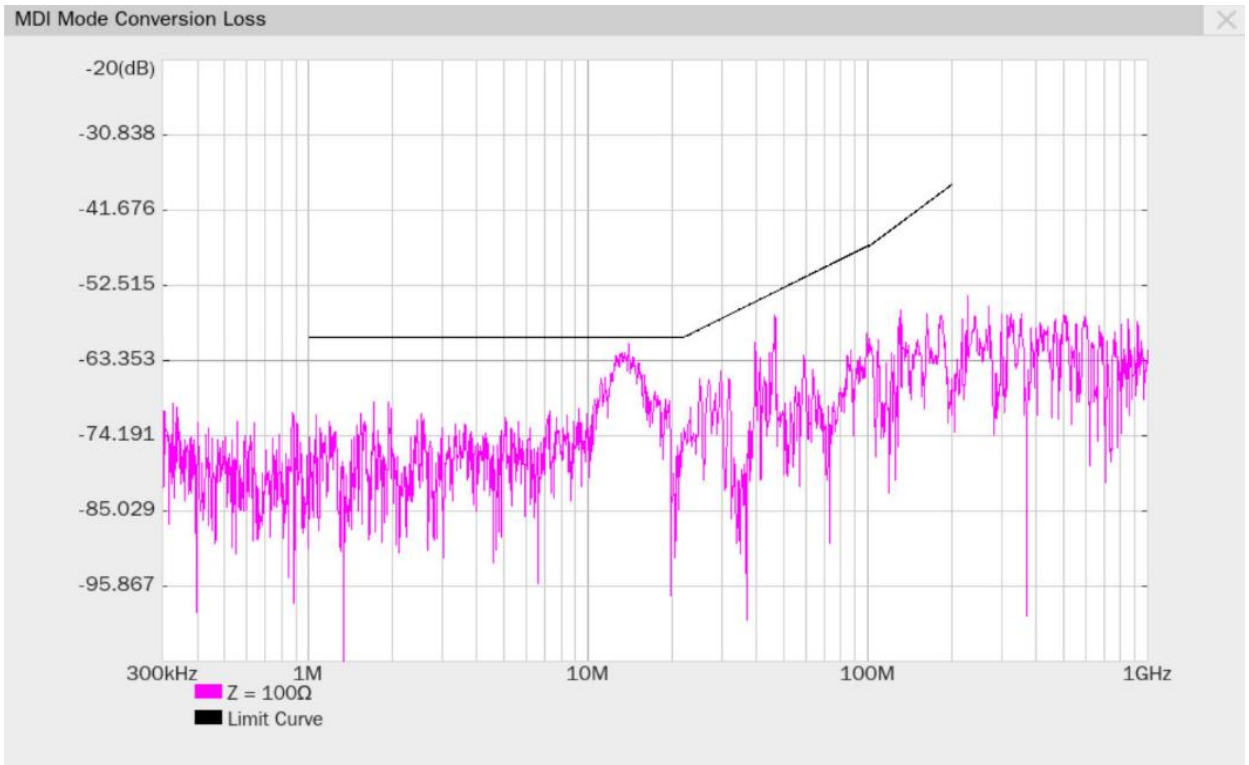


Figure 5-38 Waveform details of the MDI mode conversion loss with TC8 ECU specification

5.8 MDI Common Mode Emission Test

According to the "OABR_PMA_TX07: Check MDI Common Mode emission" section on the TC8 "OPEN Alliance Automotive Ethernet ECU Test Specification", the DUT is configured to output Test Mode 5 signal, and the MDI common mode emission should be less than 24dBuV under the terminators on the MDI interface and test fixture are matched to 100Ω in the 1MHz to 200MHz frequency range.

5.8.1 Test Environment and Connectivity

For the MDI common mode Emission test, there are two setups, which are using an Oscilloscope (shown in Figure 5-39) or a spectrum analyzer (shown in Figure 5-40) to do the test.

Note: Any other test fixture/adapter can also be used but it must meet the conditions described in the IEEE 100Base-T1 EMC Test Specifications for Transceivers, Appendix D, D.1.

5.8.1.1 Use the Oscilloscope for MDI Common Mode Emission Test

Using an Oscilloscope for MDI common mode emission test is shown in Figure 5-39. The connection is as follows:

(1) Solder the cable of DUT to TP1 on section ⑥ of the test fixture.

(2) Use one SMA cable to connect the J3 connector on the test fixture to one input channel of the Oscilloscope which is selected as the DUT “Source” channel in the user interface’s **Configure** tab.

Note: Please ensure the cable from DUT to the TP1 is as short as possible, which will get higher accuracy measurement results.

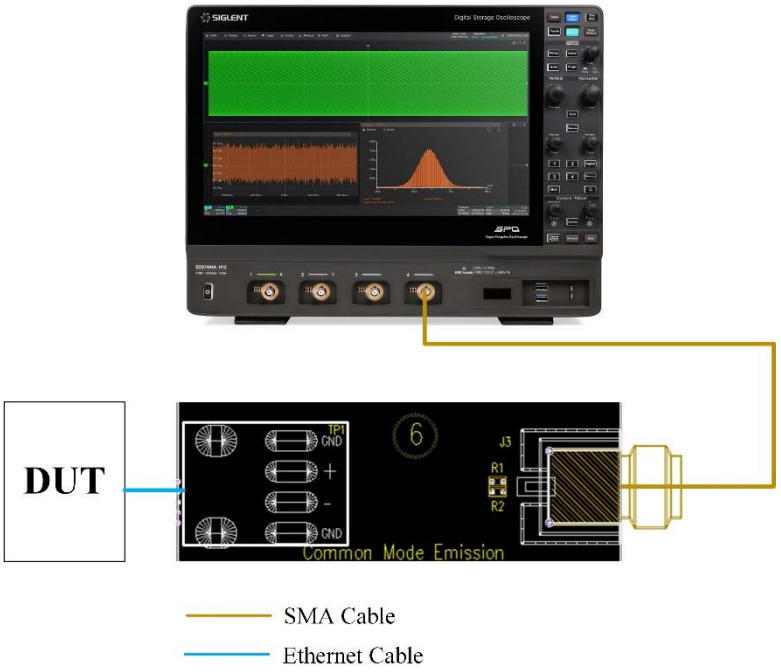


Figure 5-39 Connection for MDI common mode emission test by using the Oscilloscope

5.8.1.2 Use the Spectrum Analyzer for MDI Common Mode Emission Test

A Spectrum Analyzer can be used to run the MDI common mode emission test to achieve higher measurement accuracy compared to the Oscilloscope, connection for MDI common Mode emission test is shown in Figure 5-40. The measurement procedure is as follows:

(1) Solder the cable of DUT to TP1 on section ⑥ of the test fixture.

(2) Use a USB cable to connect the USB Host port on the Oscilloscope to the USB Device port on the Spectrum Analyzer.

(3) Use a SMA cable to connect the J3 connector on section ⑥ of the test fixture to the RF INPUT port on the Spectrum Analyzer.

(4) In the user interface's **Test Select** tab of the Oscilloscope, click **MDI Common Mode Emission**. In the **Configure** tab, click **MDI Common Mode Emission** -> **Spectrum Analyzer** -> **Connect Test**, the Oscilloscope will detect the Spectrum Analyzer connection status, if the Spectrum Analyzer is detected, then the Model Name of Spectrum Analyzer will appear, and the Oscilloscope will automatically carry out the Spectrum Analyzer setting (automatically setting only supports Siglent's model). The following is a list of Spectrum Analyzer setup:

- Measurement Unit: dBuV
- Frequency range:1MHz to 200MHz
- RBW: 10kHz
- VBW: ≥30kHz
- Detector: Positive Peak
- Frequency Sweep time: ≥20s

- Preamp: On

Note: Please ensure the cable from DUT to the TP1 is as short as possible, which will get higher accuracy measurement results.

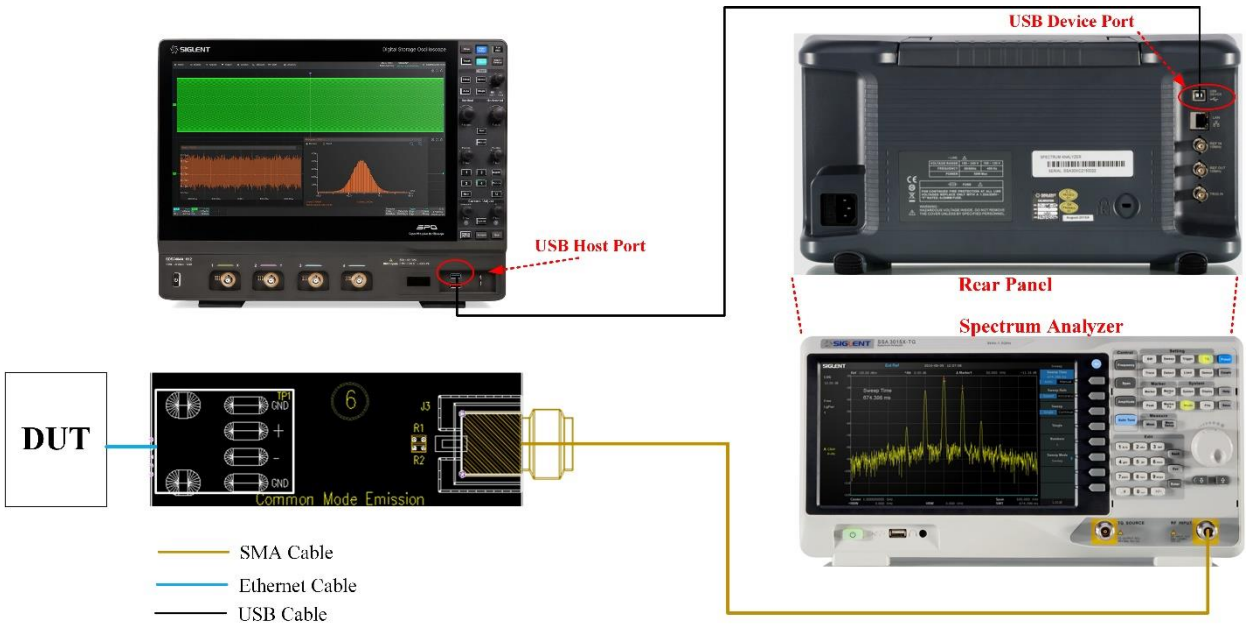


Figure 5-40 Connection for MDI common mode emission test by using the Spectrum Analyzer

5.8.2 Test procedure

(1) Configure the DUT to output test mode 5 signal.

(2) Select **OPEN Alliance** specification for the compliance test in **Setup** tab.

(3) Select the **MDI Common Mode Emission** In the **Test Select** tab.

(4) Select the **Oscilloscope** or **Spectrum Analyzer** in the **Configure** tab and set the pass or fail limit, the default limit for MDI common mode emission test is 24dBuV.

(5) Check the correctness of the test environment setup in the **Connect** tab.

(6) Click **Run Test** .

(7) If the system is not physically configured to perform this test, the application will return to the **Connect** step to prompt you to change the physical configuration. When you have completed these instructions, click **Run Test** button to resume the test run.

(8) During the test, if you choose to use the Oscilloscope to do the test, then the Oscilloscope will automatically verify whether the correct test signal is present on the configured DUT “Source” channel, if effective signal is detected, the Oscilloscope will configure the correct trigger level to capture the signal. After finishing the test, the Oscilloscope will output the test results.

If you choose to use the Spectrum Analyzers to measure the MDI common mode emission test, the Oscilloscope will control the Spectrum analyzers to perform the measurements and plot the

curve according to the Spectrum analyzers' measurement then output the test results.

5.8.3 Algorithm

According to the section "OABR_PMA_TX07" in the of "OPEN Alliance Automotive Ethernet ECU Test Specification", in the frequency range of 1MHz~200MHz, the threshold of MDI common mode emission is 24dBuV. When the common mode emission of the DUT is less than 24dBuV, then the test passes.

5.8.4 Test Result Reference

The test result of the MDI common mode emission is shown in Figure 5-41. The waveform details are shown in Figure 5-42.

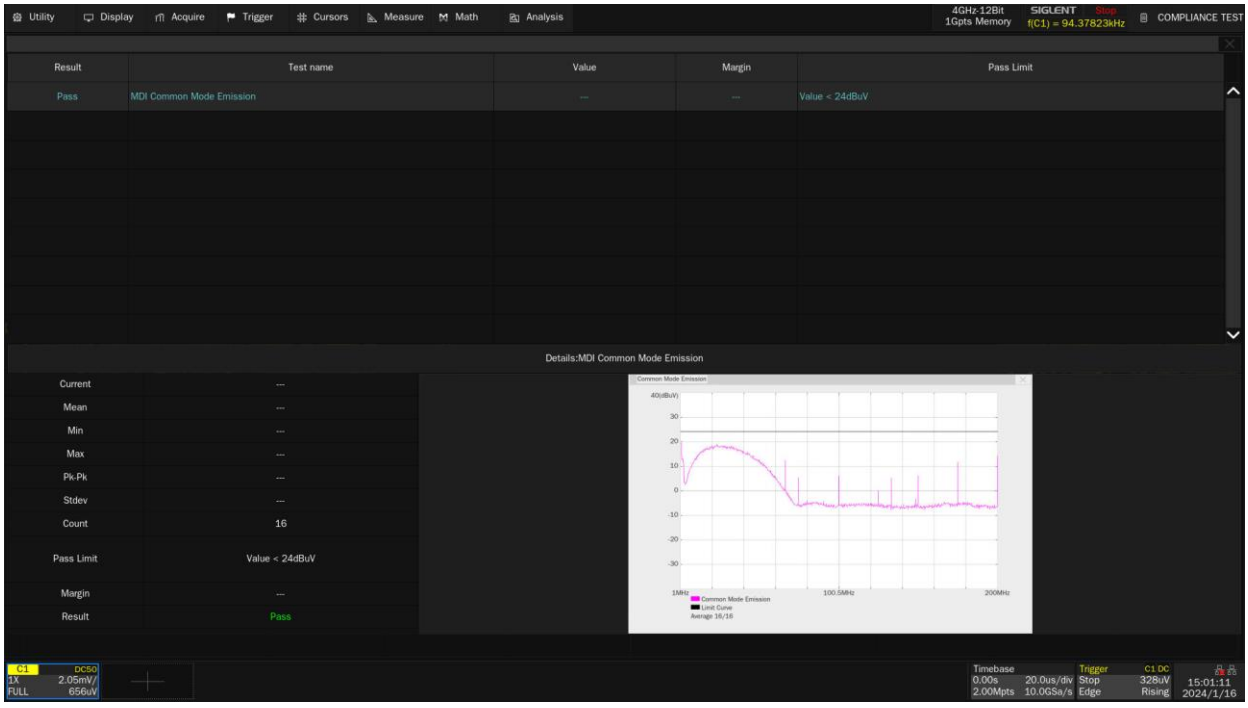


Figure 5-41 Test result of the MDI common mode emission

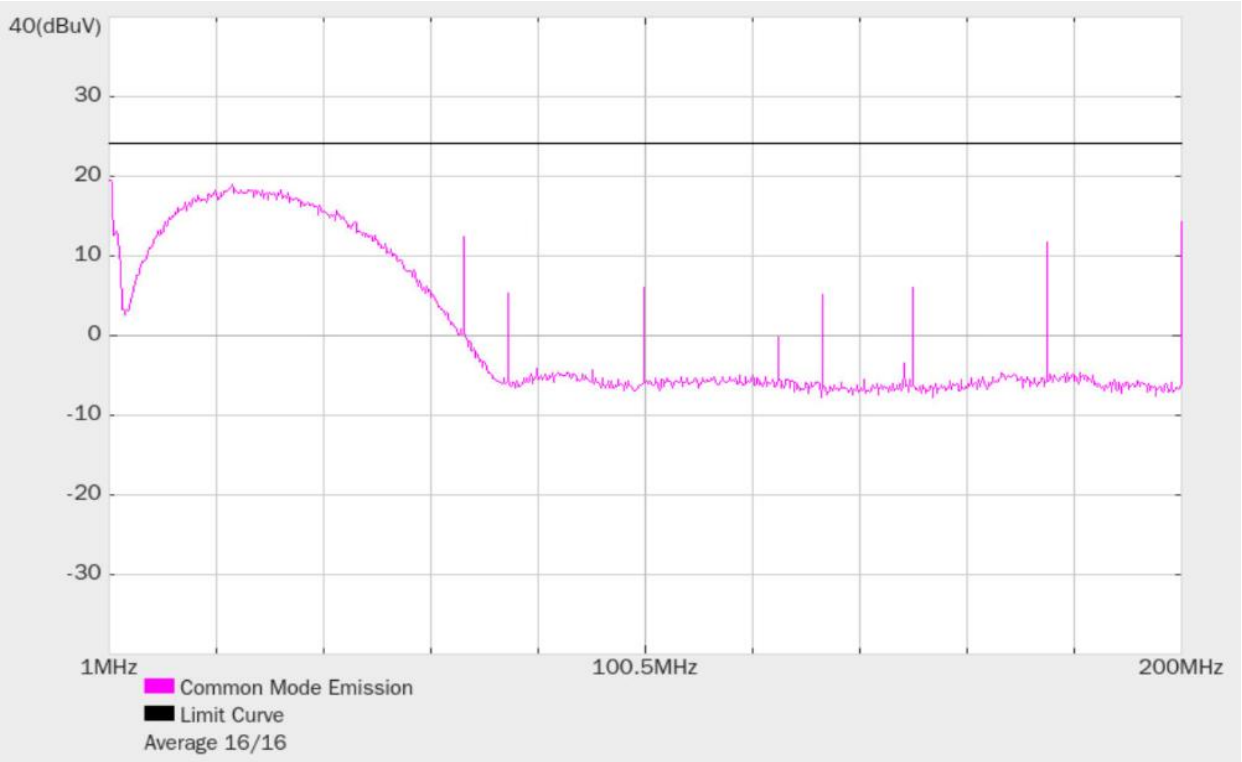


Figure 5-42 Waveform details of the MDI common mode emission

6 1000BASE-T1 Compliance Tests

6.1 TX_TCLK125 Frequency and Jitter Tests

According to Section 97.5.2 of IEEE Std 802.3bp specification, when the DUT is in test mode 1, the PHY shall provide access to a frequency reduced version of the transmit symbol clock or TX_TCLK125. This 125MHz test clock is one-sixth frequency divided version of TX_TCLK that times the transmitted symbols.

The Section 97.5.3.6 of IEEE Std 802.3bp specification specifies the symbol transmission rate of the Master PHY shall be within the range of 750MHz±100ppm. For the compliance PHY, the symbol transmit rate is 750 MHz ± 100 ppm, so 1/6 of the symbol transmit clock frequency which is measured should be in the range of 125 MHz ± 100 ppm.

The Section 97.5.3.3 of IEEE Std 802.3bp specification specifies the value of the TX_TCLK125 jitter.

6.1.1 Test Environment and Connectivity

According to the Figure 97-31 in Section 97.5.2.1 of IEEE Std 802.3bp specification, which is shown in Figure 6-1, connect the DUT with Link Partner, the link is up between DUT and Link Partner and two PHYs have established up(link status is set to OK), then connect the TX_TCLK125 clock signal of the DUT directly to the Oscilloscope to test the frequency and jitter when the DUT is in Master or Slave mode.

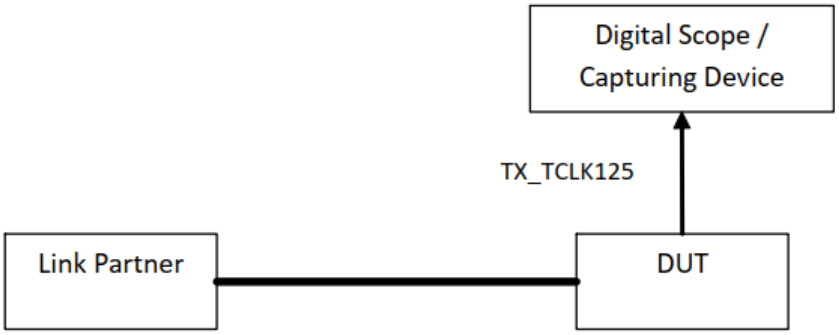


Figure 97–31—Transmitter test fixture 3 for MASTER and SLAVE clock jitter measurement

Figure 6-1 TX_TCLK125 frequency and jitter measurement setup for Master and Slave mode

The connection on SDS7000A is the same as Figure 6-1, which is used to test the frequency and jitter of the TX_TCLK125 of the DUT, please refer to Figure 6-2.

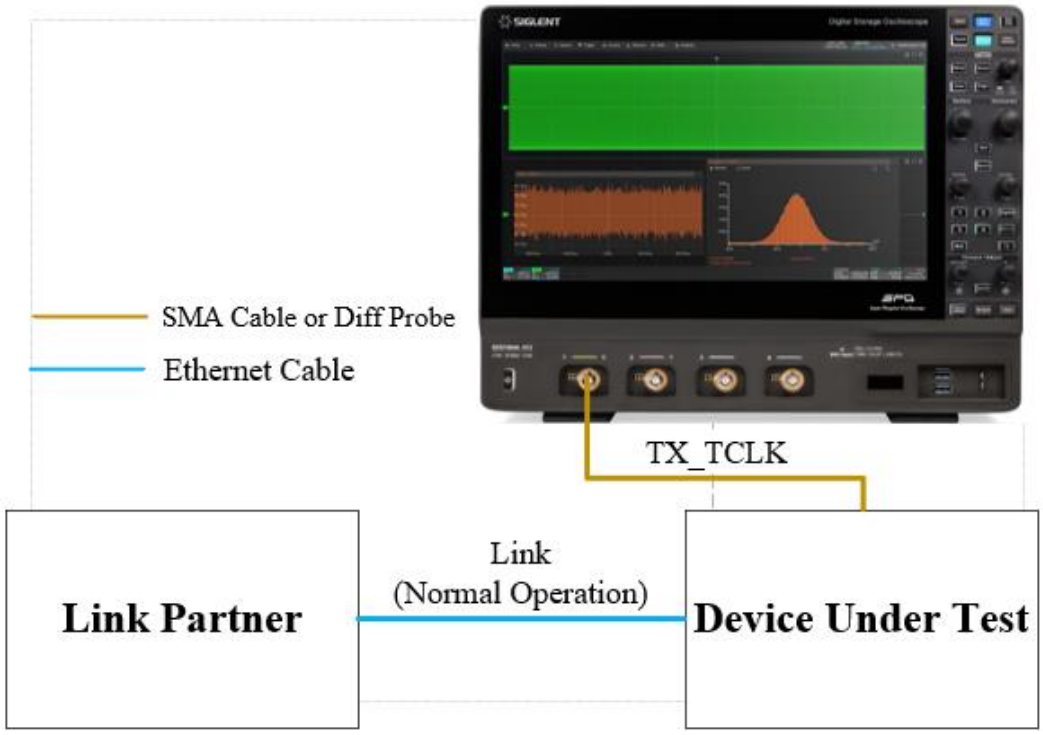


Figure 6-2 TX_TCLK125 frequency and jitter measurement setup for Master and Slave mode on SDS7000A

6.1.2 Test Procedure

(1) Configure the DUT to output test mode 1 signal. Ensure that the link between DUT and Link Partner is in normal operation.

(2) Select the **TX_TCLK125 Frequency and Jitter** In the **Test Select** tab.

(3) Set the source channel, input impedance, average number, edge and bandpass filter in the **Configure** tab.

(4) Check the correctness of the test environment setup in the **Connect** tab.

(5) Click **Run Test** .

(6) If the system is not physically configured to perform this test, the application will return to the **Connect** step to prompt you to change the physical configuration. When you have completed these instructions, click **Run Test** button to resume the test run.

(7) During the test, the Oscilloscope will automatically verify whether the correct test signal is present on the configured DUT “Source” channel, if effective signal is detected, the Oscilloscope will configure the correct trigger level to capture the signal. After finishing the tests, the Oscilloscope will output the test results.

6.1.3 Algorithm

Test Mode 1 enables testing of frequency and timing jitter on Master and Slave transmitters. Connect Master and Slave transmitters over a link segment. The transmitter timing jitter is measured by capturing the TX_TCLK125 waveforms in both Master and Slave configurations.

Section 97.5.3.6 of the IEEE Std 802.3bp specification specifies that the compliant PHY should have a symbol transmission rate of 750 MHz ± 100 ppm.

Section 97.5.2 of the IEEE Std 802.3bp specification specifies that when in Test Mode 1, the 1000BASE-T1 PHY shall provide access to a frequency reduced version of the transmit symbol clock or TX_TCLK125. This 125 MHz test clock is one sixth frequency divided version of TX_TCLK that times the transmitted symbols.

Section 97.5.3.3 of the IEEE Std 802.3bp specification specifies that for the compliant PHY, when the DUT is in Master mode, the RMS value of the TX_TCLK125 jitter relative to an unjittered reference shall be less than 5 ps, and the peak-to-peak value of the jitter relative to an unjittered reference shall be less than 50 ps. When the DUT is in Slave mode, the RMS value of the TX_TCLK125 jitter relative to an unjittered reference shall be less than 10 ps, and the peak-to-peak value of the jitter relative to an unjittered reference shall be less than 100 ps.

6.1.4 Test Results Reference

The test results of the TX_TCLK125 frequency and jitter are shown in Figure 6-3. The waveform details are shown in Figure 6-4.

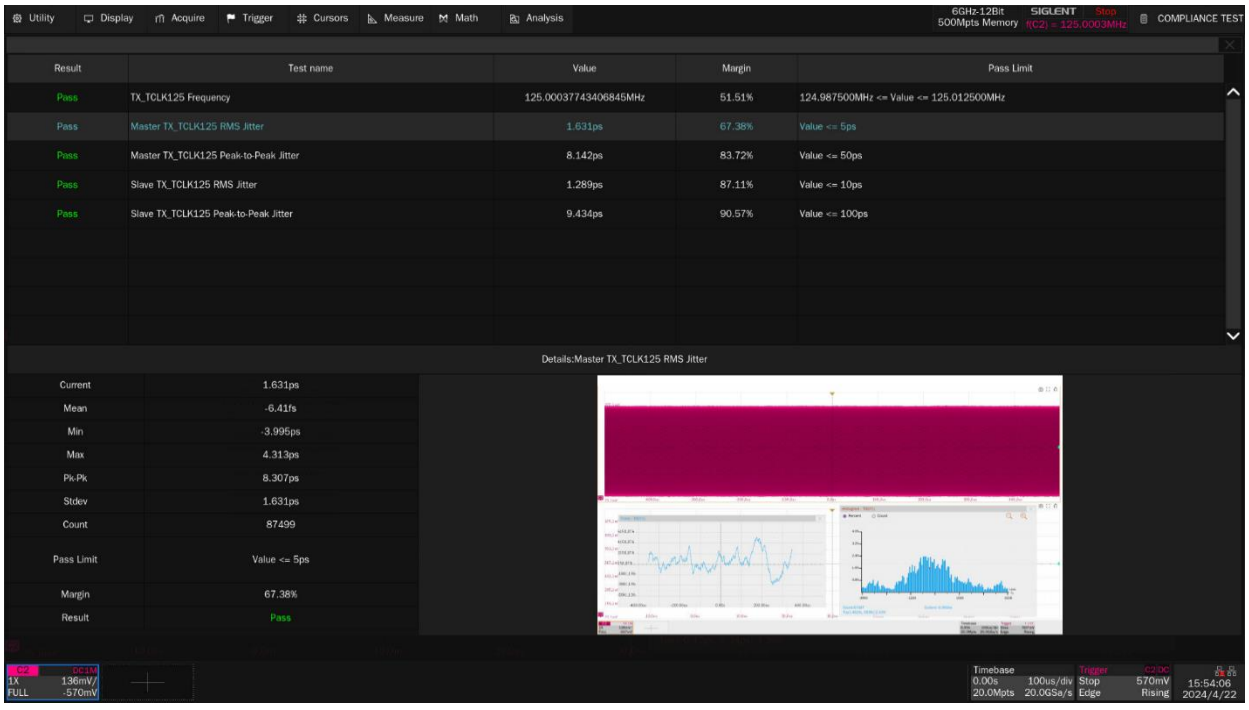


Figure 6-3 Test results of the TX_TCLK125 frequency and jitter

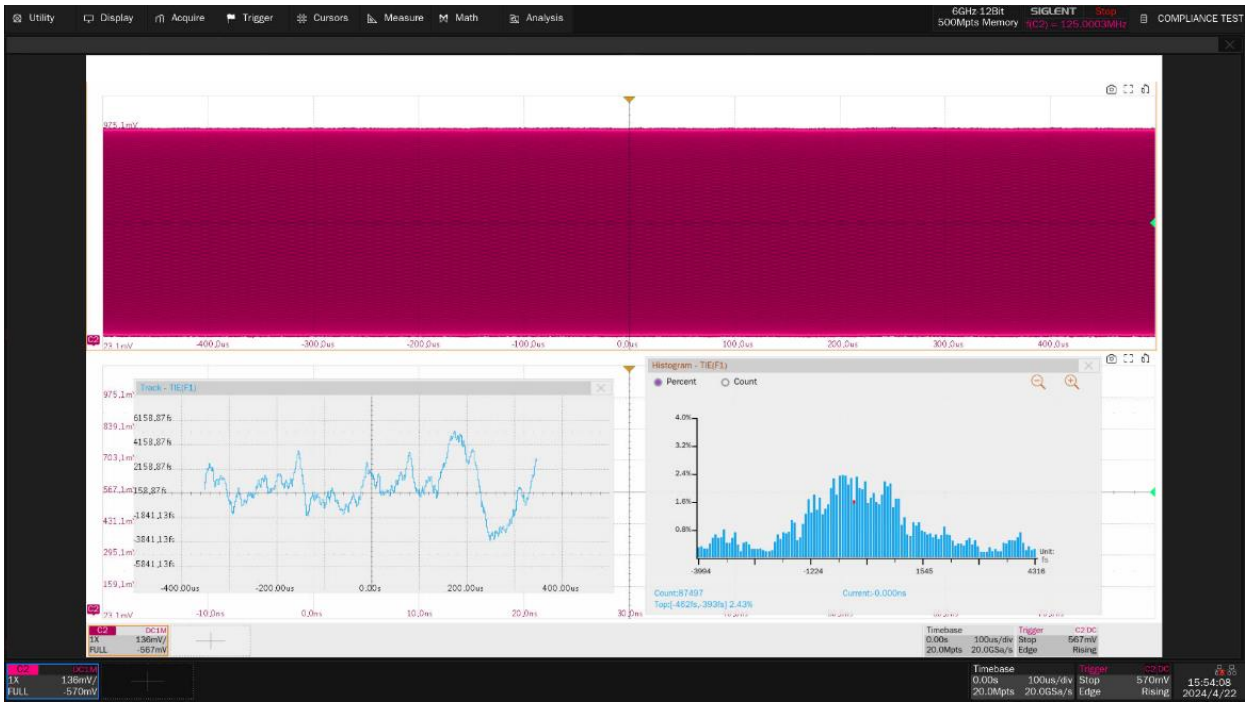


Figure 6-4 Waveform details of the TX_TCLK125 jitter

6.2 Transmit Clock Frequency and MDI Output Jitter Tests

These tests are measuring the transmit clock frequency and MDI timing jitter when DUT is in Test Mode 2.

Test mode 2 is for transmitter timing jitter test on MDI when transmitter is in Master timing mode. When test mode 2 is enabled, the 1000BASE-T1 PHY shall transmit a continuous pattern of three {+1} symbols followed by three {–1} symbols with the transmitted symbols timed from its local clock source of 750 MHz, the transmitter output is a 125 MHz ± 100 ppm signal.

The RMS value of the transmit clock jitter relative to an unjittered reference shall be less than 5 ps, the peak-to-peak value of the jitter relative to an unjittered reference shall be less than 50 ps.

6.2.1 Test Environment and Connectivity

A pair of SMA cables or an active differential probe can be used to probe the signal.

The connection by using a pair of SMA cables is shown in Figure 6-5. The connection procedure is as follows:

(1) Use two SMA cables with equal length to connect the test points J1(+) and J4(-) on section ④ of the test fixture, and to two input channels which are selected as the DUT “Source” channels in the user interface’s **Configure** tab.

(2) Solder the Ethernet cable of the DUT to TP2 on the test fixture.

(3) A cable tie can be used to fasten the Ethernet cable to the through-hole.

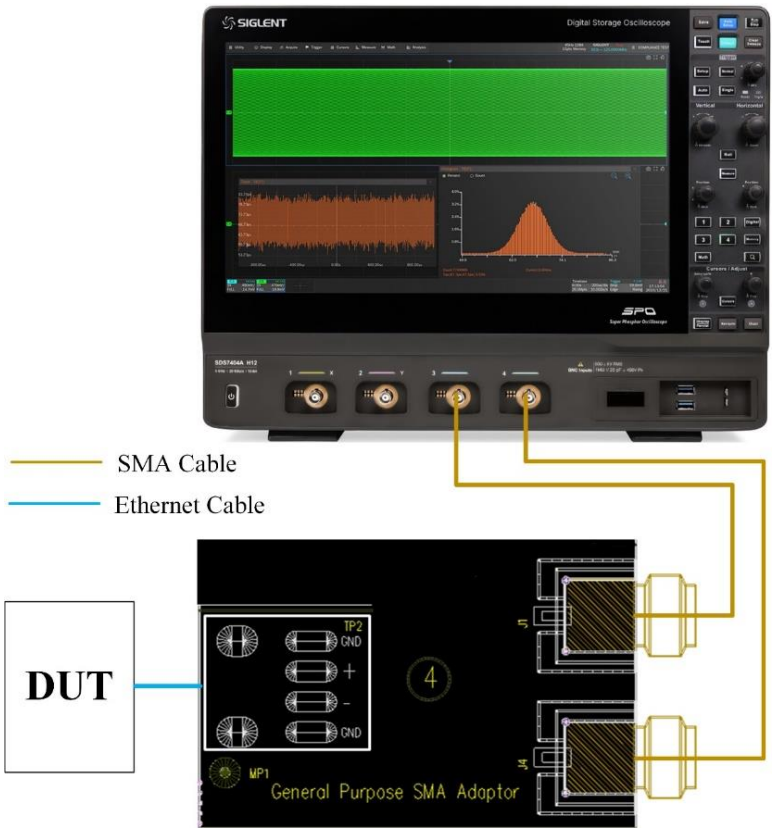


Figure 6-5 Connection to the Oscilloscope by using a pair of SMA cables

The connection by using an active differential probe is shown in Figure 6-6. The connection procedure is as follows:

(1) Connect an active differential probe to the test point J17 on section ① of the test fixture, and to the Oscilloscope input channel which is selected as the DUT “Source” channel in the user interface’s **Configure** tab.

(2) Solder the Ethernet cable of the DUT to TP4 on the test fixture.

(3) Ensure correct polarity of the probe head.

(4) A cable tie can be used to fasten the Ethernet cable to the through-hole.

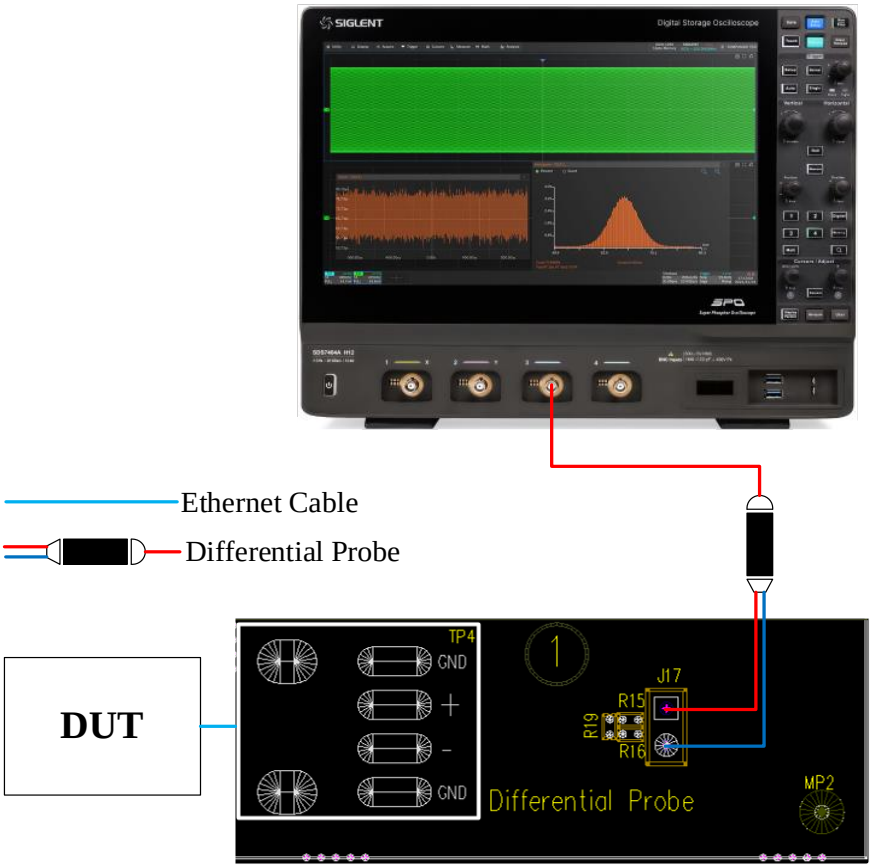


Figure 6-6 Connection to the Oscilloscope by using a Differential Probe

6.2.2 Test Procedure

(1) Configure the DUT to output test mode 2 signal.

(2) Select the **Transmit Clock Frequency and MDI Output jitter** in the **Test Select** tab.

(3) Set the probe type (differential probe or single-ended input), source channel, average number, edges and bandpass filter in the **Configure** tab.

(4) Check the correctness of the test environment setup in the **Connect** tab.

(5) Click **Run Test** .

(6) If the system is not physically configured to perform this test, the application will return to the **Connect** step to prompt you to change the physical configuration. When you have completed these instructions, click **Run Test** button to resume the test run.

(7) During the test, the Oscilloscope will automatically verify whether the correct test signal is present on the configured DUT “Source” channel, if effective signal is detected, the Oscilloscope will configure the correct trigger level to capture the signal. After finishing the tests, the Oscilloscope will output the test results.

6.2.3 Algorithm

Section 97.5.3.6 of the IEEE Std 802.3bp specification specifies that the compliant PHY should have a symbol transmission rate of 750 MHz ± 100 ppm.

Section 97.5.2 of the IEEE Std 802.3bp specification specifies that when in Test Mode 2, the 1000BASE-T1 PHY shall transmit a continuous pattern of three {+1} symbols followed by three {–1} symbols with the transmitted symbols timed from its local clock source of 750 MHz. Therefore, the signal frequency tested at the MDI shall be 125MHz± 100 ppm.

Section 97.5.3.3 of the IEEE Std 802.3bp specification specifies that for the compliant PHY, when the DUT is in Test Mode 2, the RMS value of the MDI output jitter relative to an unjittered reference shall be less than 5 ps, and the peak-to-peak value of the MDI output jitter relative to an unjittered reference shall be less than 50 ps.

The jitter measurement can respond to the time interval error (TIE) of the data on MDI. The Oscilloscope calculates the ideal reference from the measured data and compares it to the original signal to determine the data time interval error.

6.2.4 Test Results Reference

The test results of the transmit clock frequency and MDI output jitter are shown in Figure 6-7. The waveform details are shown in Figure 6-8.

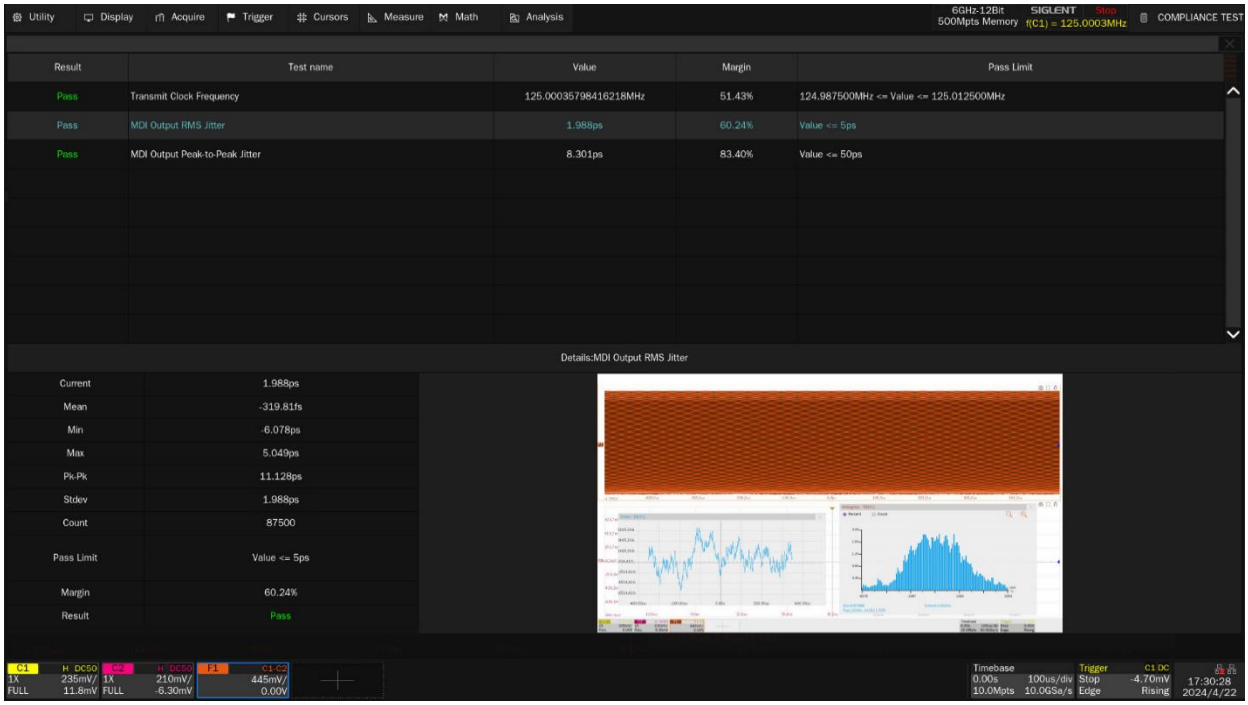


Figure 6-7 Test results of the transmit clock frequency and MDI output jitter

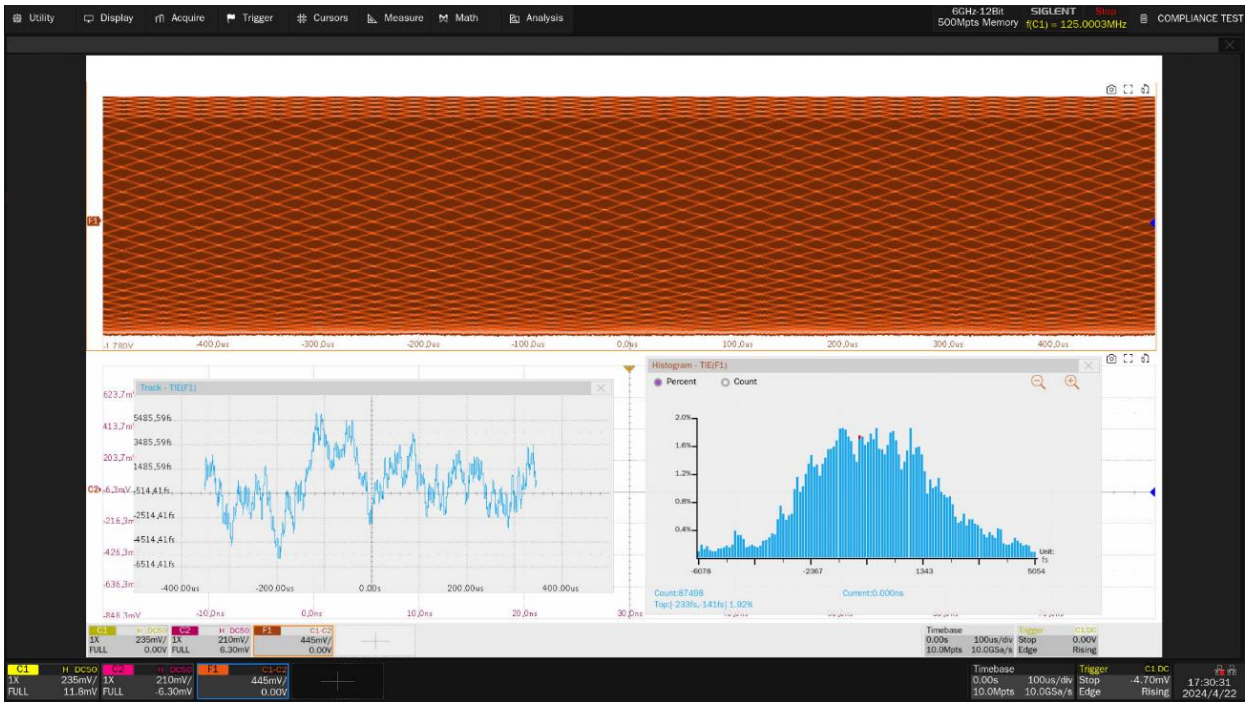


Figure 6-8 Waveform details of the MDI output jitter

6.3 Transmitter Distortion Test

According to Section 97.5.3.2 of the IEEE Std 802.3bp specification, the DUT continuous sends out many blocks of 2047 defined symbols after it enters into Test Mode 4. Section 97.5.3.2 of the specification provides MATLAB code to analyze transmission distortion. The peak distortion values, measured at a minimum of 10 equally spaced phases of a single symbol period, shall be less than 15 mV.

6.3.1 Test Environment and Connectivity

The configuration of the transmitter distortion on the SDS7000A Oscilloscope is shown in Figure 6-9. Siglent's transmitter distortion test supports the use of Arbitrary Waveform Generator to output disturbing signal to the DUT for distortion test.

Alternatively, you can also run this test without the disturbing signal, but you cannot use the result to determine compliance. By this way, the user can uncheck the **Disturbing Signal** to do the transmitter distortion test.

In order to improve the accuracy of transmitter distortion test, you need to check **TX_TCLK125** in the configure tab. Then connect **TX_TCLK125** of the DUT to the input interface of the Frequency Converter test fixture, the test fixture will generate two identical 10MHz clock signals from TX_TCLK125, both of the 10MHz clock output needed to connect to the external clock source ports of the Oscilloscope and the Disturber. By this way the clock domain synchronization among the DUT, Oscilloscope and Arbitrary Waveform Generator can be achieved.

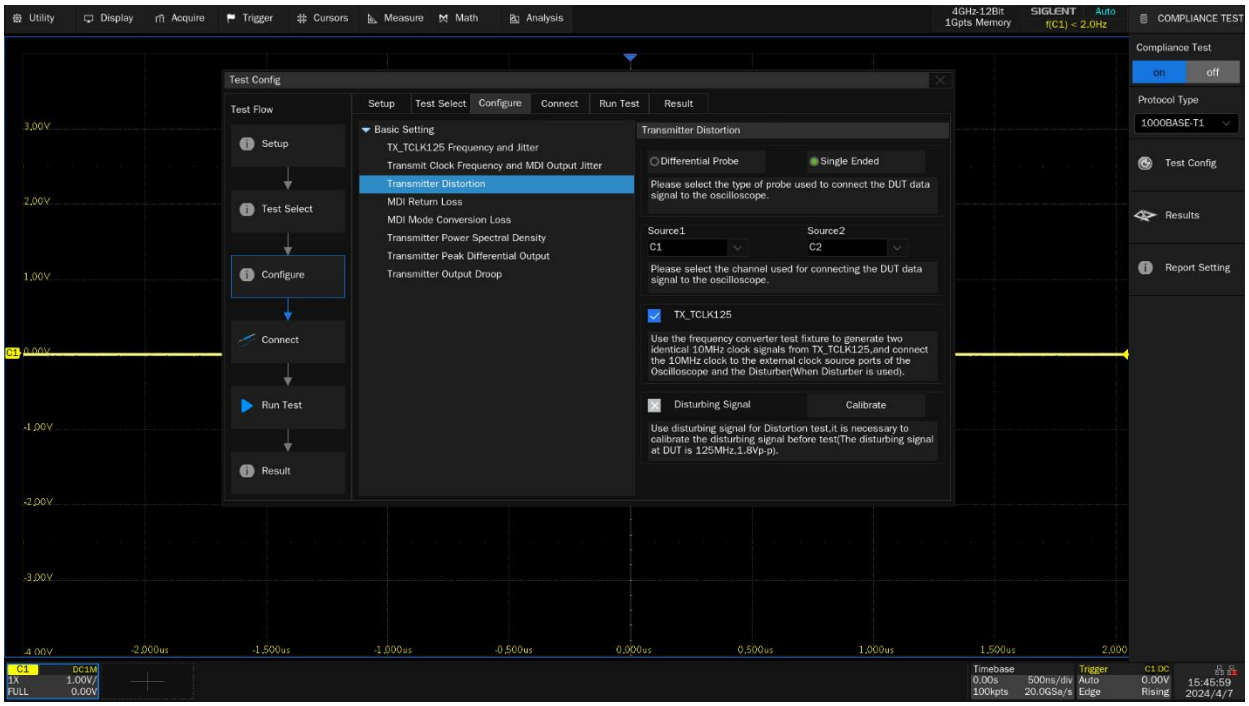


Figure 6-9 Configuration of transmitter distortion test

6.3.1.1 Disturbing Signal Path Calibration

After checking **TX_TCLK125** and **Disturbing Signal**, it is necessary to calibrate the disturbing signal path before performing the transmitter distortion test, the calibration environment and connection is shown in Figure 6-10. The calibration procedure for disturbing signal path is as follows:

(1) The connection between Frequency Converter and test equipment is as follows:

1) Supply a DC5V power to the Frequency Converter test fixture through J6 or J9 connector, the HL3 and HL5 LED will light up.

2) Connect the DUT's TX_TCLK125 to the J1(CH1) or J2(CH2) input channel on the Frequency Converter test fixture. Install a jumper on J5(pin 1,2) to select CH2 as the input channel (CH2 input impedance is 50ohm); Install a jumper on J5(pin 2,3) to select CH1 as the input channel (CH1 input impedance is 10kohm).

3) Input clock frequency selection: place the jumper on J7(pin2,3) to indicates the input clock frequency of TX_TCLK125 is 125MHz.

4) Check the frequency lock indicator: When HL2 lights up, which means that the frequency conversion from 125MHz to 10MHz works well. When HL2 is off, it means that the PLL chip is not locked, you need to check whether the input clock, J5 and J7 are configured correctly or not. When the configuration is correct, the user can press the Reset Button S1 or power on the Frequency Converter again.

5) Connect J3(Clock Output: CH1) and J12(Clock Output: CH2) to the external clock source ports of the Oscilloscope and Arbitrary Waveform Generator respectively.

6) Set the clock source of the Oscilloscope and Arbitrary Waveform Generator to external.

(2) Use section ② on the Automotive Ethernet Test Fixture to do the disturbing signal calibration. The connection is shown as follows:

1) J5, J14 connectors are installed with 50ohm terminators.
2) Connect the J2 and J8 connectors on the test fixture to two input channels on the Oscilloscope which are selected as the DUT's "Source" channels in the user interface's **Configure** tab with equal length cables.
3) Connect the J15 and J16 connectors on the test fixture to two output channels on the Disturber.
4) Set the Disturber to output two sine wave signals with the same amplitude but with a 180° phase shift. The sine wave frequency is 125MHz, which is exactly 1/6 of the transmission symbol rate.
5) Set the input impedance of the Oscilloscope to 50Ω. The Oscilloscope subtracts two input signals and measure the peak-to-peak value of the differential signal. Continuously adjust the output amplitude of the Disturber until the peak-to-peak voltage reads to 1.8V_{p-p}. Record and save the Disturber setting for the following transmitter distortion tests.

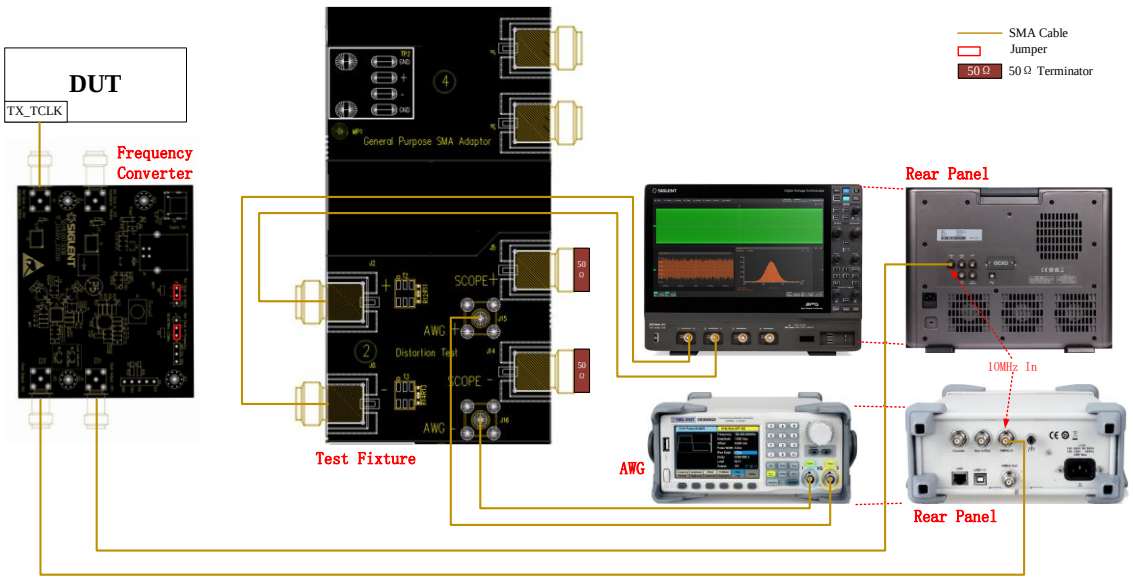


Figure 6-10 Calibration environment and connection for disturbing signal

6.3.1.2 Environment Setup for Transmitter Distortion Test

The transmitter distortion test can be performed with or without disturbing signal. Please setup the test environment according to requirements. But you cannot use the result to determine compliance without disturbing signal.

A. With TX_TCLK125 clock and with disturbing signal

The connection with TX_TCLK125 and with disturbing signal is shown in Figure 6-11. The test procedure is shown as follows:

(1) Configure the DUT to output Test Mode 4 signal.

(2) The connection between Frequency Converter and test equipment is as follows:

1) Supply a DC5V power to the Frequency Converter test fixture through J6 or J9 connector, the HL3 and HL5 LEDs will light up.

2) Connect the DUT's TX_TCLK125 to the J1(CH1) or J2(CH2) input channel on the Frequency Converter test fixture. Install a jumper on J5(pin1,2) to select CH2 as the input channel (CH2 input impedance is 50ohm); Install a jumper on J5(pin2,3) to select CH1 as the input channel (CH1 input impedance is 10kohm).

3) Input clock frequency selection: place the jumper on J7(pin 2,3) to indicates the input clock frequency of TX_TCLK125 is 125MHz.

4) Check the frequency lock indicator: When HL2 lights up, which means that the frequency conversion from 125MHz to 10MHz works well. When HL2 is off, it means that the PLL chip is not locked, you need to check whether the input clock, J5 and J7 are configured correctly or not. When the configuration is correct, you can press the Reset Button S1 or power up the Frequency Converter again.

5) Connect J3(Clock Output: CH1) and J12(Clock Output: CH2) to the external clock source ports of the Oscilloscope and Arbitrary Waveform Generator respectively.

6) Set the clock source of the Oscilloscope and Arbitrary Waveform Generator to external.

(3) On the section ② and ④ of the Automotive Ethernet Test Fixture. The connection is as follows:

1) Solder the cable of DUT to TP2 on section ④ of the test fixture.

2) On the test fixture, use two SMA cables with equal length to connect the J1(+) and J4(-) connectors on section ④ to J2(+) and J8(-) connectors on section ②.

3) Connect the J15 and J16 connectors on the test fixture to two output channels on the Disturber, with the disturbing sine wave which has been finished calibrating.

4) Connect the J5 and J14 connectors on section ② of the test fixture to two input channels on the Oscilloscope which are selected as the DUT "Source" channels in the user interface's **Configure** tab.

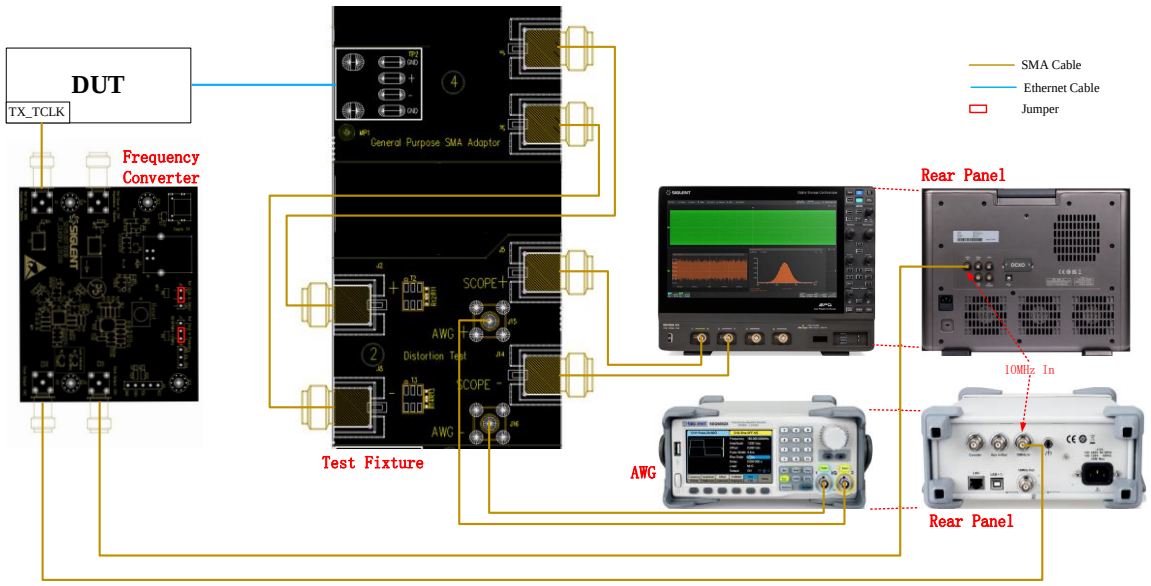


Figure 6-11 Environment setup for transmitter distortion tests by using a pair of SMA cables (with disturbing signal)

B. With TX_TCLK125 clock, without disturbing signal

(1) Configure the DUT to output Test Mode 4 signal.

(2) The connection between Frequency Converter and test equipment is as follows:

1) Supply a DC5V power to the Frequency Converter test fixture through J6 or J9 connector, the HL3 and HL5 LEDs will light up.

2) Connect the DUT's TX_TCLK125 to the J1(CH1) or J2(CH2) input channel on the Frequency Converter test fixture. Install a jumper on J5(pin1,2) to select CH2 as the input channel (CH2 input impedance is 50ohm); Install a jumper on J5(pin2,3) to select CH1 as the input channel (CH1 input impedance is 10kohm).

3) Input clock frequency selection: place the jumper on J7(pin 2,3) to indicates the input clock frequency of TX_TCLK125 is 125MHz.

4) Check the frequency lock indicator: When HL2 lights up, which means that the frequency conversion from 125MHz to 10MHz works well. When HL2 is off, it means that the PLL chip is not locked, you need to check whether the input clock, J5 and J7 are configured correctly or not. When the configuration is correct, you can press the Reset Button S1 or power up the Frequency Converter again.

5) Connect J3(Clock Output: CH1) or J12(Clock Output: CH2) to the external clock source port of the Oscilloscope.

6) Set the clock source of the Oscilloscope to external.

(3) On the section ④ of the Automotive Ethernet Test Fixture. The connection is as follows:

1) Solder the cable of DUT to TP2 on section ④ of the test fixture.

2) Use two SMA cables with equal length to connect the J1(+) and J4(-) connectors on section ④ of the test fixture to two input channels on the Oscilloscope which are selected as the DUT "Source" channels in the user interface's **Configure** tab.

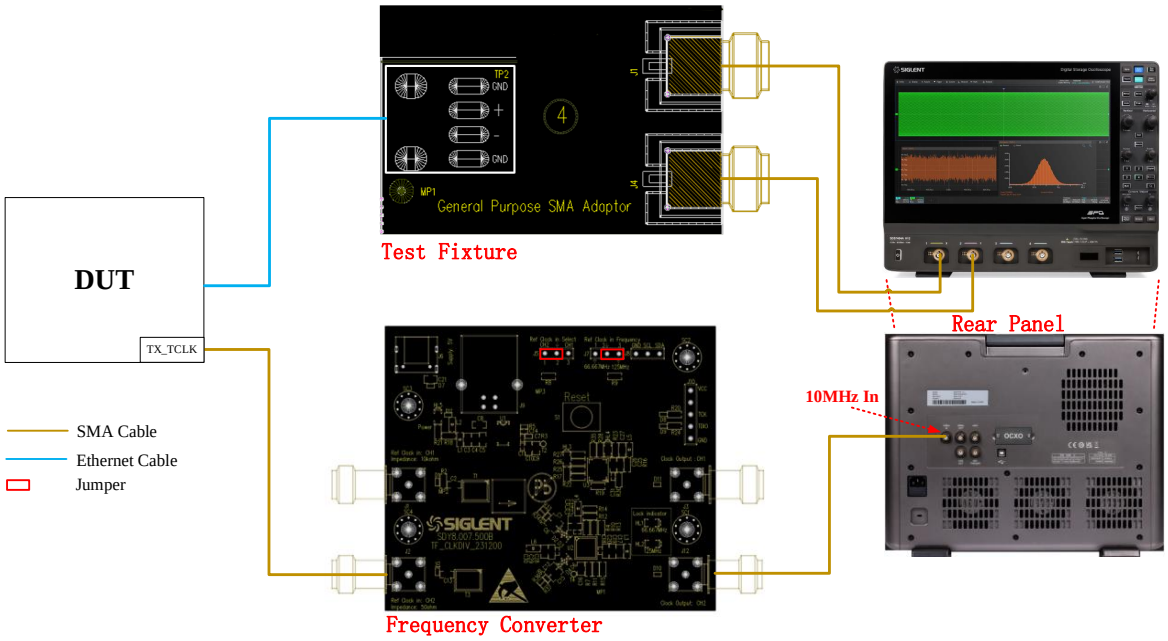


Figure 6-12 Environment setup for transmitter distortion tests by using a pair of SMA cables (without disturbing signal)

The test environment and connection for transmitter distortion test with Frequency Converter and with an active differential probe but without the disturbing signal is shown as Figure 6-13. The test procedure is similar with the distortion test by using a pair of SMA cables.

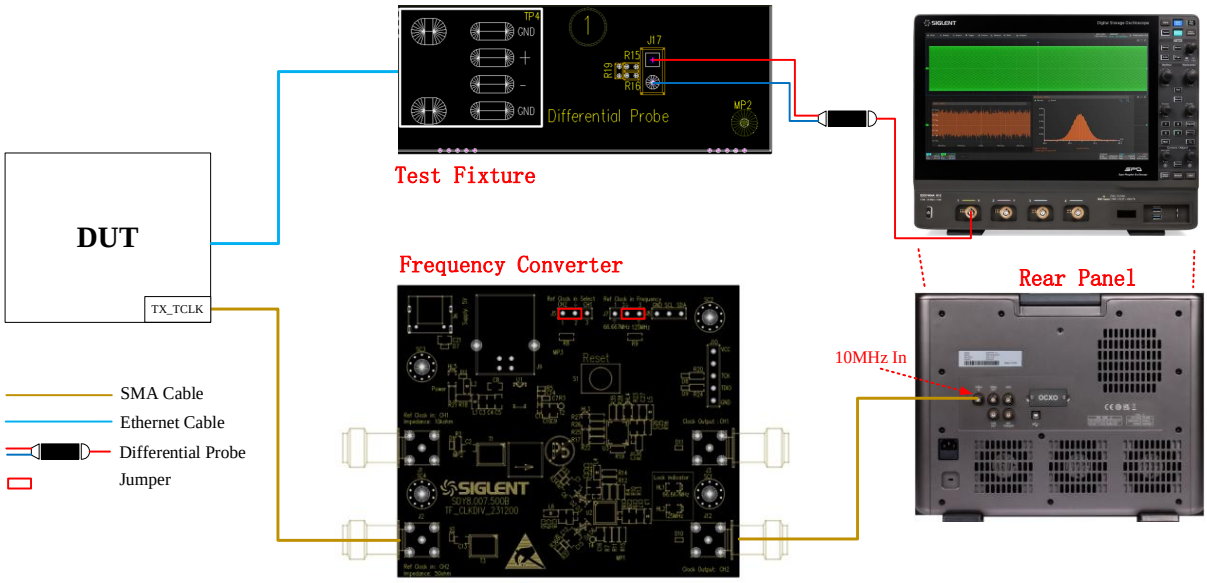


Figure 6-13 Environment setup for transmitter distortion test by using a differential probe (without disturbing signal)

6.3.2 Test Procedure

(1) Configure the DUT to output test mode 4 signal.

(2) Select the **Transmitter Distortion** In the **Test Select** tab.

(3) Set the probe type (differential probe or single-ended input), source channel, with or without disturbing signal in the **Configure** tab.

(4) Check the correctness of the test environment setup in the **Connect** tab.

(5) Click **Run Test** .

(6) If the system is not physically configured to perform this test, the application will return to the **Connect** step to prompt you to change the physical configuration. When you have completed these instructions, click **Run Test** button to resume the test run.

(7) During the test, the Oscilloscope will automatically verify whether the correct test signal is present on the configured DUT “Source” channel, if effective signal is detected, the Oscilloscope will configure the correct trigger level to capture the signal. After finishing the tests, the Oscilloscope will output the test results.

6.3.3 Algorithm

The transmitter distortion test is according to the section 97.5.3.2 of IEEE Std 802.3bp specification.
The specifications specify that the Oscilloscope and Arbitrary Waveform Generator are synchronized by the TX_TCLK125 clock of the DUT. the peak distortion is determined by sampling the differential signal output with the symbol rate clock at an arbitrary phase and processing a block of any 2047 consecutive samples with MATLAB code provide in IEEE Std 802.3bp.
The peak distortion values, measured at a minimum of 10 equally spaced phases of a single symbol period, shall be less than 15 mV.
Alternatively, you can run transmitter distortion test without disturbing signal, but the test result is only for informative purpose and it cannot be used to determine the compliance.

6.3.4 Test Result Reference

The transmitter distortion test result is shown in Figure 6-14.

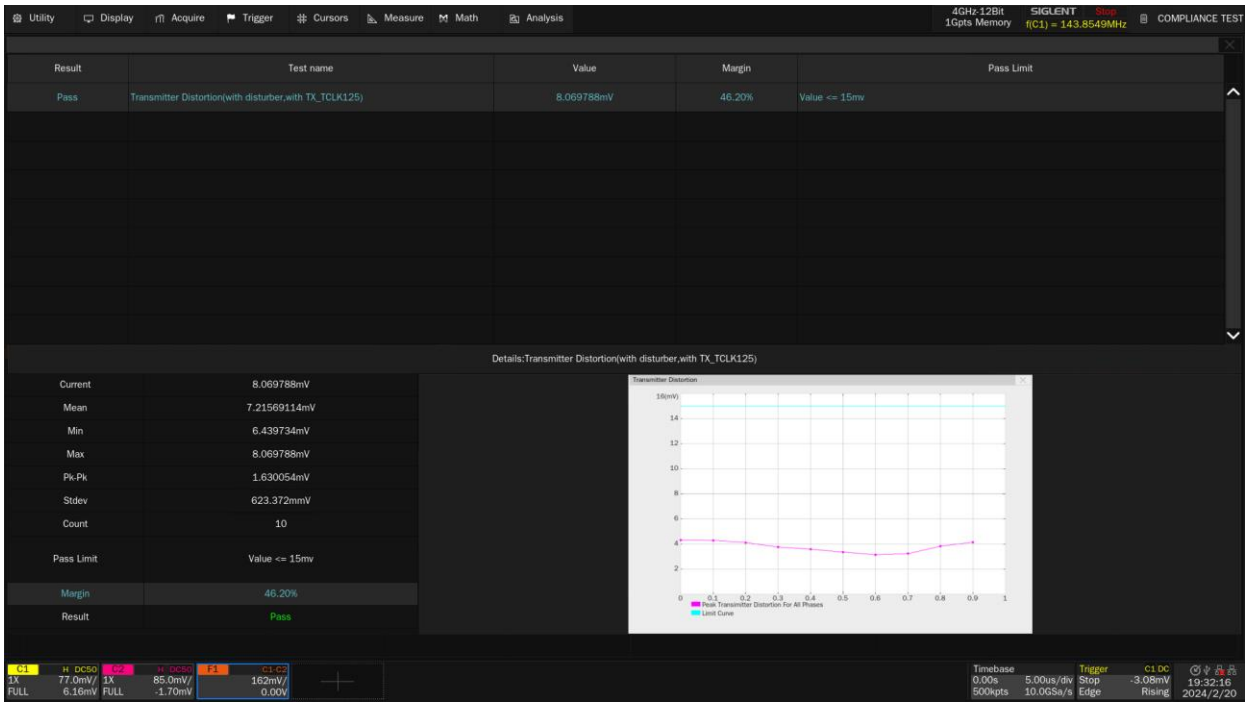


Figure 6-14 Transmitter distortion test result

The details of the test waveform for transmitter distortion test are shown in Figure 6-15.

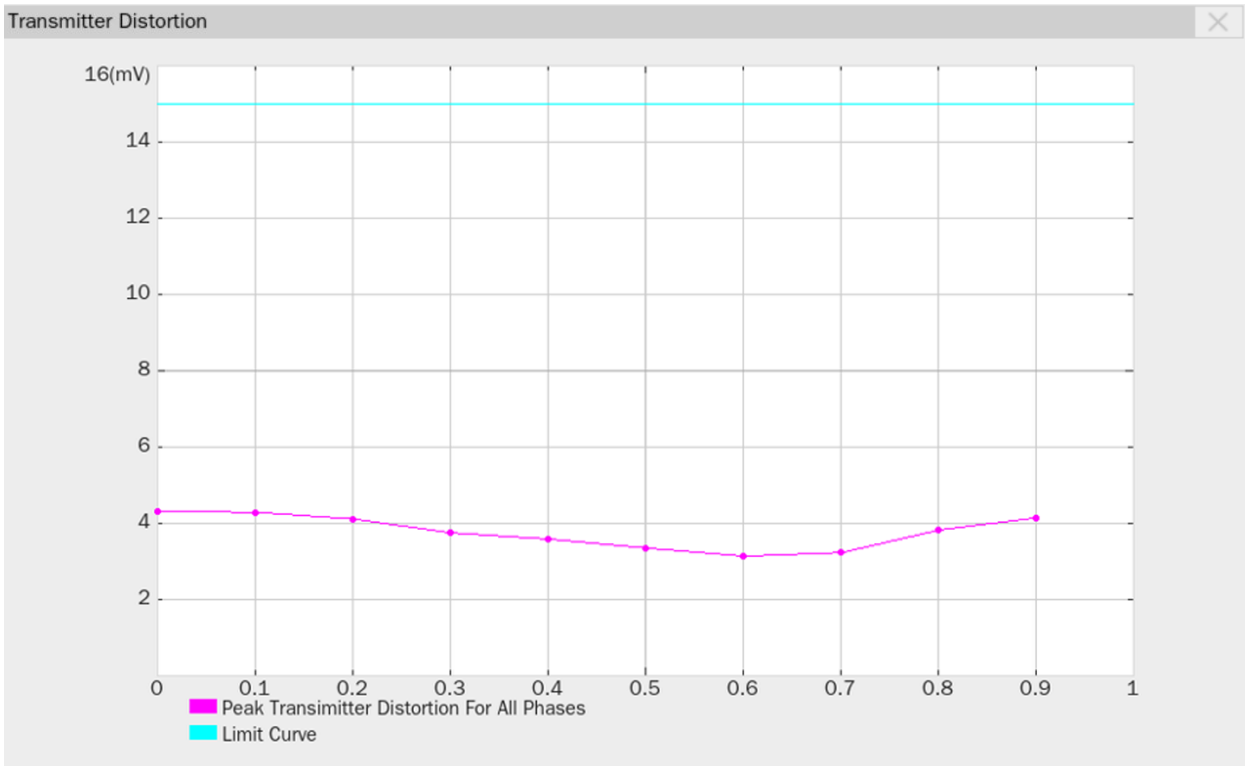


Figure 6-15 Waveform details for transmitter distortion test

6.4 MDI Return Loss Test

The Section 97.7.2.1 of IEEE Std 802.3bp specification specifies that when doing the MDI return loss test, the DUT must be configured in Slave mode and not transmit any test symbols, the MDI return loss shall be within the specification among 2MHz to 600MHz frequency range with 100Ω differential impedance termination.

6.4.1 Test Environment and Connectivity

The VNA needs to be calibrated before the running the MDI return loss test.

6.4.1.1 VNA Calibration

For the MDI return loss test, the VNA needs to be calibrated before measuring the MDI return loss, the calibration environment uses two ports on VNA which is shown in Figure 6-16.

Steps for VNA calibration is performed as follows:

(1) Use a USB cable to connect the USB Host port on the Oscilloscope to the USB Device port on the VNA.

(2) Use two SMA cables with equal length to connect two Ports of the VNA, and to the Calibration Kit.

(3) In the user interface's **Test Select** tab of the Oscilloscope, click **MDI Return Loss**. In the **Configure** tab, click **Connect Test**, the Oscilloscope will detect the VNA connection status, if the VNA is detected, then the Model Name of VNA will appear, and the Oscilloscope will automatically carry out the VNA setting (automatically setting only supports Siglent's model). The following is a list of VNA setup:

- Measurement: Return Loss（Sdd11）
- Start frequency: 2MHz
- Stop frequency: 600MHz
- Sweep type: Logarithmic
- Sweep points: 1601
- Output power: -10dBm(min), 0dBm (Recommended)
- IF Bandwidth: 100Hz
- Logic port impedance differential mode: 100Ω
- Logic port impedance common mode: 25Ω
- Smooth function is deactivated

(4) In the **Configure** -> **MDI Return Loss**, set the measurement type to **Balanced Measure**.

(5) Set the calibration parameters of VNA for Open, Load, Short and Through calibration.

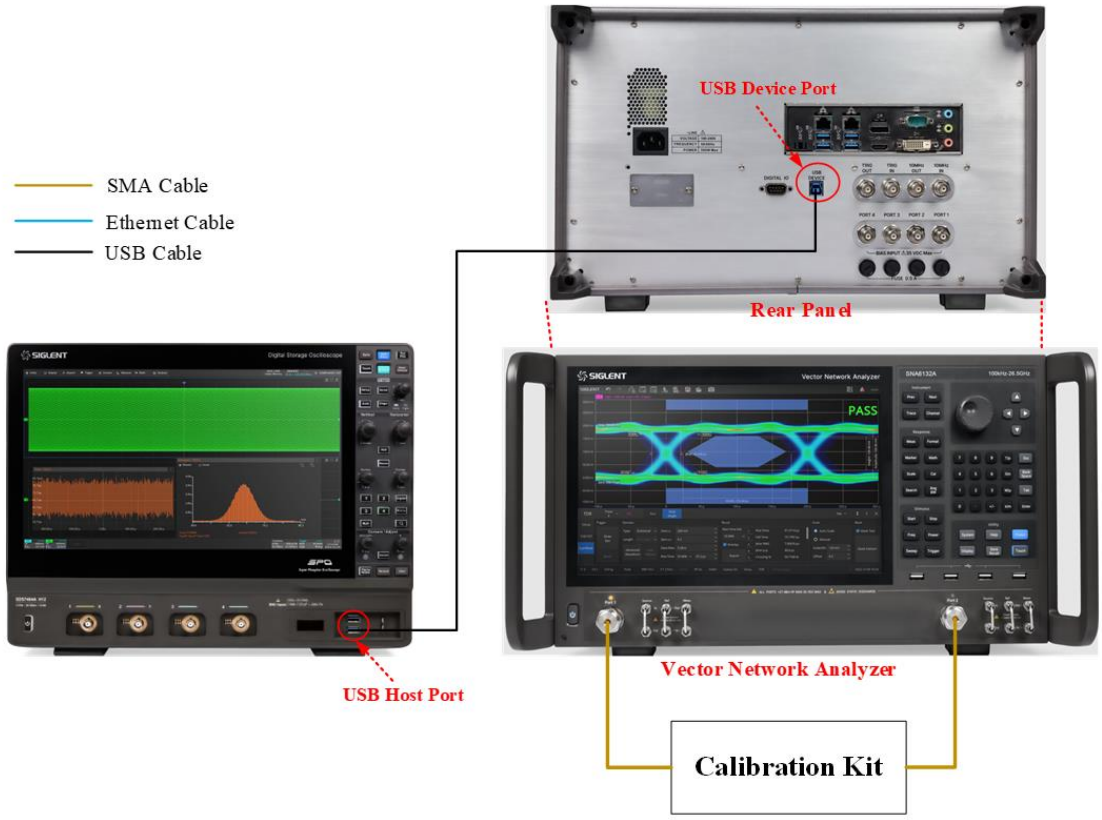


Figure 6-16 Calibration environment for return loss by using Balanced Measure method

6.4.1.2 Test Environment for MDI Return Loss

The test environment for the MDI return loss by using balanced measurement method is shown Figure 6-17. The test procedure is as follows:

(1) The DUT must be set to Slave Mode of operation and not transmitting any test symbols.

(2) Use two SMA cables with equal length to connect the test points J1(+) and J4(-) on section ④ of the test fixture, and to two ports on the VNA which are selected for measurement.

(3) Solder the cable of DUT to TP2 on section ④ of the test fixture.

(4) Use a USB cable to connect the USB Host port on the Oscilloscope to the USB Device port on the VNA.

(5) In the **Configure** -> **MDI Return Loss**, set the measurement type to **Balanced Measure**.

(6) On the Oscilloscope Click **Run Test**, and check the correctness of the test environment setup before click **Run Test** when the pop-up window appears. The Oscilloscope will automatically acquire the return loss data tested by the VNA and plots the curve, and outputs the test result.

Note: Please ensure the cable from DUT to the TP2 is as short as possible, which will get higher measurement accuracy results.

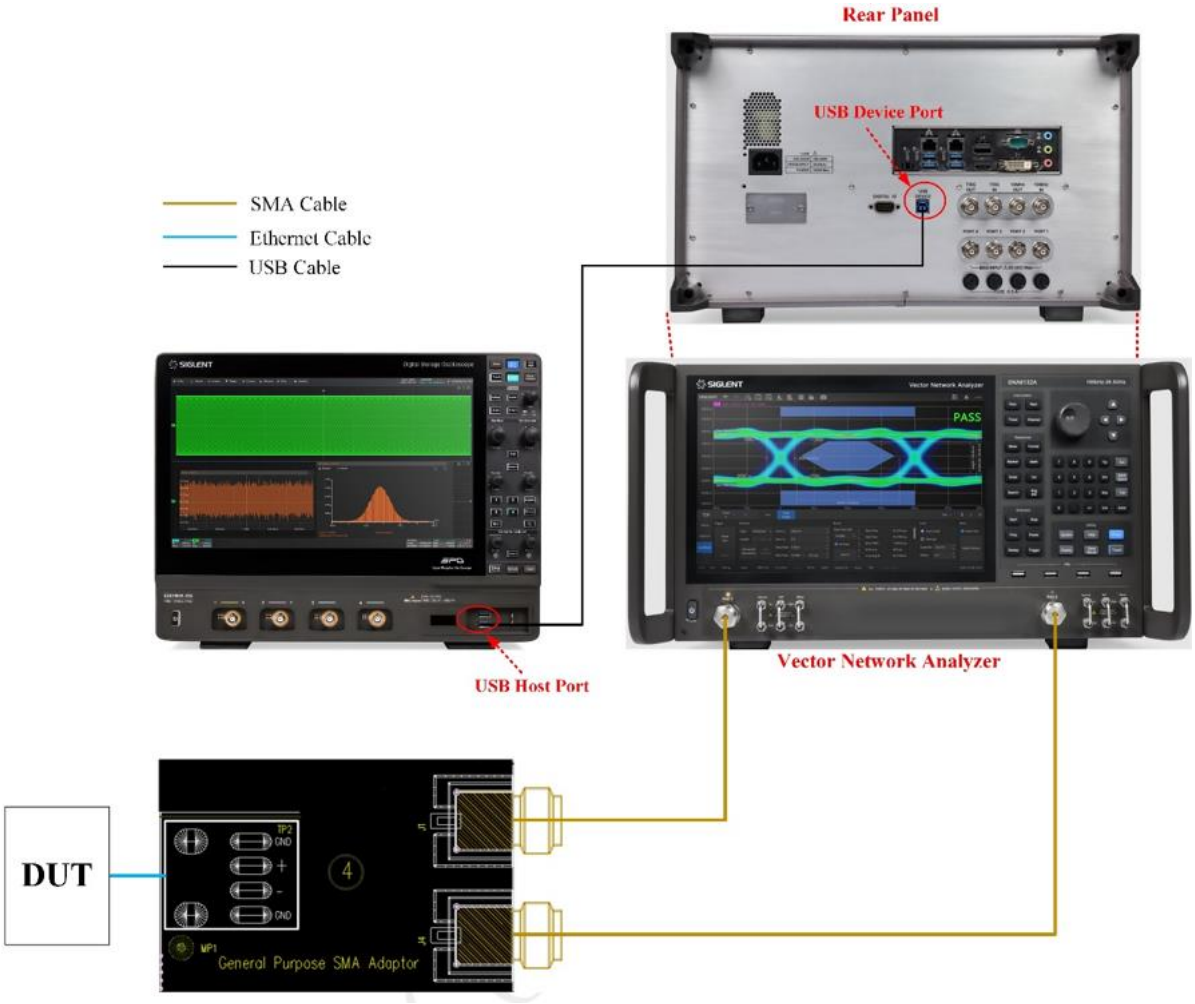


Figure 6-17 Connection for MDI return loss using balanced measurements

6.4.2 Test Procedure

(1) The DUT must be set to Slave Mode and not transmitting any test symbols.

(2) Select **MDI Return Loss** In the **Test Select** tab.

(3) In the **Configure** tab, click **Connect Test**, the Oscilloscope will detect the VNA connection status, if the VNA is detected, then the Model Name of VNA will appear

(4) in the **Configure** tab, select **Balanced Measure** .

(5) Check the correctness of the test environment setup in the **Connect** tab. The VNA should be finished calibrating before doing the MDI return loss test.

(6) Click **Run Test** .

(7) If the system is not physically configured to perform this test, the application will return to the **Connect** step to prompt you to change the physical configuration. When you have completed these instructions, click **Run Test** button to resume the test run.

(8) During the test, the Oscilloscope will automatically control the VNA to perform the MDI return loss measurements and plot the curve according to the VNA's measurement then output the test results.

6.4.3 Algorithm

Section97.7.2.1 of the IEEE Std 802.3bp specification specifies that, the differential impedance at the MDI for each transmit/receive channel shall be such that any reflection (due to differential signals incident upon the MDI with a test port having a differential impedance of 100 Ω) is attenuated relative to the incident signal as follows:

- MDI return loss should be larger than $18-18\times\log_{10}(20/f)$ dB in the frequency range of 2MHz to 20MHz.
- MDI return loss should be larger than 18 dB in the frequency range of 20MHz to 100MHz.
- MDI return loss should be larger than $18-16.7\times\log_{10}(f/100)$ dB in the frequency range of 100MHz to 600MHz.

6.4.4 Test Result Reference

The test result of the MDI return loss is shown in Figure 6-18. The waveform details are shown in Figure 6-19.

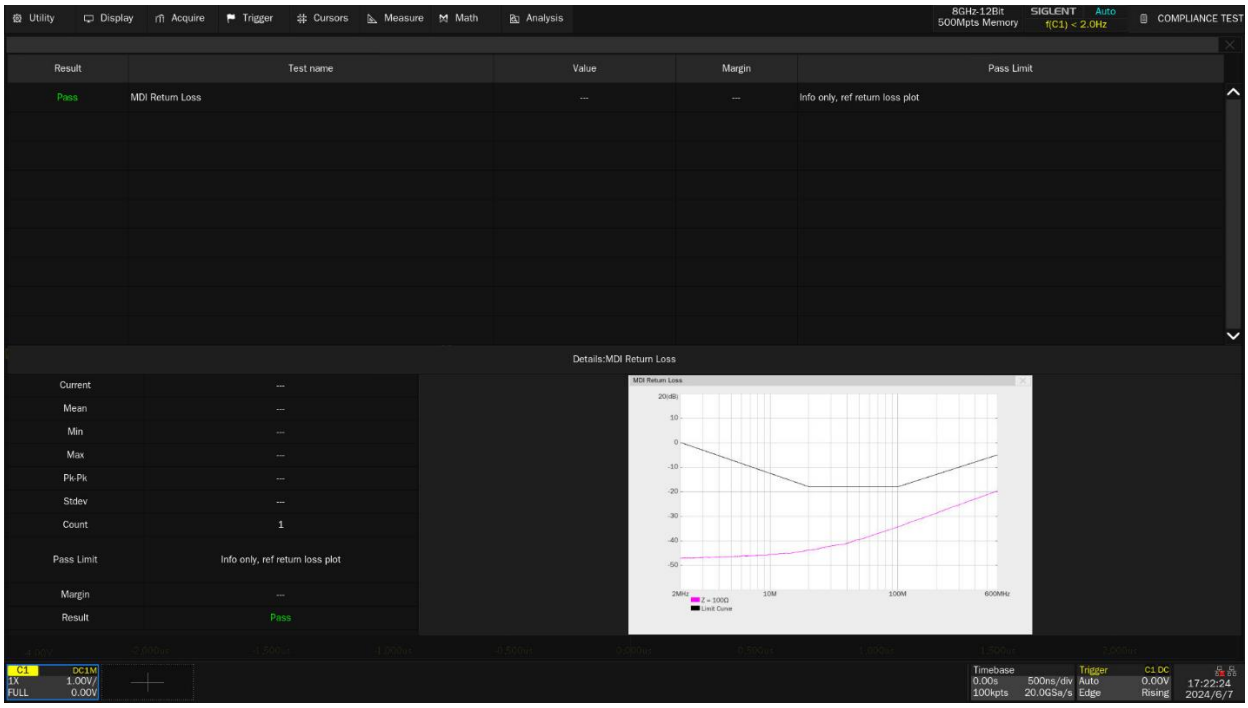


Figure 6-18 Test result of the MDI return loss

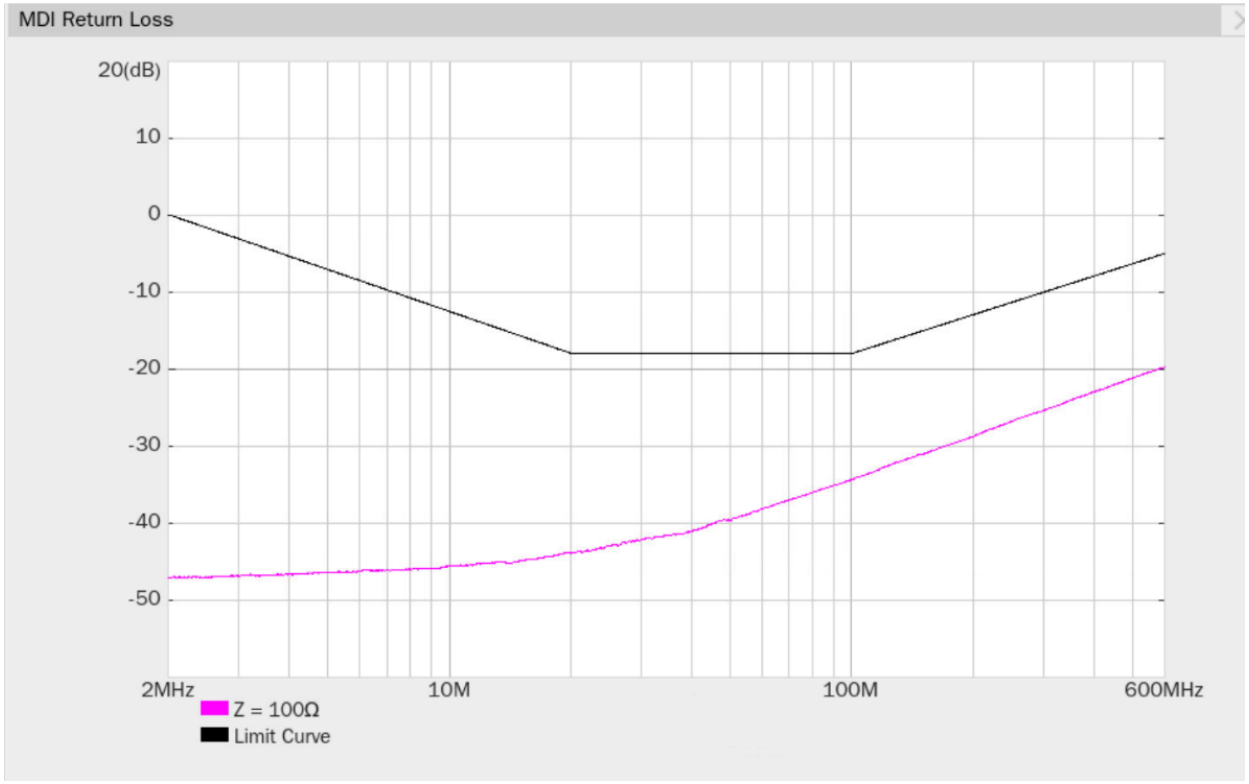


Figure 6-19 Waveform details of the MDI return loss

6.5 MDI Mode Conversion Loss Test

Section 97.7.2.2 of the IEEE Std 802.3bp specification specifies that the MDI mode conversion loss (Sdc11: common mode to differential mode conversion) of the transmitter (with 100 Ω impedance termination) shall be within the limits at all times when the PHY is transmitting data or control symbols from 10MHz to 600MHz frequency range.

When doing the MDI mode conversion loss test, the DUT must be configured in Slave mode and not transmit any test symbols.

6.5.1 Test Environment and Connectivity

The VNA needs to be calibrated before running the MDI mode conversion loss test, after calibration the mode conversion loss test can be performed.

The VNA calibration and test environment for 1000BASE-T1 MDI mode conversion loss are the same as <6.4.1 Test Environment and Connectivity> chapter, which requires two ports on the VNA for the test.

The VNA calibration can be used the SOLT or SOLR calibration method. But the TRL can achieve very high precision because the two-port TRL calibration method does not need to know the index parameters of the calibration kit, and all the error items in the error model of the test device can be figured out through three simple connection methods. TRL calibration scheme will use the THRU

straight through calibration element, reflection calibration kit (Open or Short), and a small section of transmission line. Through TRL calibration method, the measurement error due to the test fixture can be minimized.

Note: If the LINE standard of appropriate length or loss cannot be fabricated, a MATCH standard maybe used instead of the LINE. The MATCH standard may be defined as an infinite length transmission line OR as a 1-port low reflect termination, such as a load.

The user can set the calibration parameters of VNA for Open, Load, Short and Through calibration with the SOLT or SOLR calibration method. But the Reflect, Through, Line calibration with the RTL calibration method can achieve higher calibration precision.

Calibrate the VNA before the tests. Set the VNA as follows:

- Measurement: Mode Conversion (Sdc11)
- Start frequency: 10MHz
- Stop frequency: 600MHz
- Sweep type: Logarithmic
- Sweep points: 1601
- Output power: -10dBm(min), 0dBm (Recommended)
- IF Bandwidth: 100Hz
- Logic port impedance differential mode: 100Ω
- Logic port impedance common mode: 25Ω
- Smooth function is deactivated

6.5.2 Test Procedure

(1) The DUT must be set to Slave Mode and not transmitting any test symbols.

(2) Select the **MDI Mode Conversion Loss** In the **Test Select** tab.

(3) In the **Configure** tab, click **Connect Test**, the Oscilloscope will detect the VNA connection status, if the VNA is detected, then the Model Name of VNA will appear

(4) Check the correctness of the test environment setup in the **Connect** tab. The VNA should be finished calibrating before doing the MDI mode conversion loss test.

(5) Click **Run Test** .

(6) If the system is not physically configured to perform this test, the application will return to the **Connect** step to prompt you to change the physical configuration. When you have completed these instructions, click **Run Test** button to resume the test run.

(7) During the test, the Oscilloscope will automatically control the VNA to perform the MDI mode conversion loss measurements and plot the curve according to the VNA's measurement then output the test results.

6.5.3 Algorithm

Section 97.7.2.2 of the IEEE Std 802.3bp specification specifies that, the MDI Mode Conversion Loss shall meet or better than the following equation for all frequencies ranging from 10 MHz to 600 MHz at all times when the PHY is transmitting data or control symbols, the limit is shown in Figure 6-20.

- MDI Sdc11 should be smaller than -55 dB in the frequency range of 10MHz to 80MHz.
- MDI Sdc11 should be smaller than -(77-11.51×$\log_{10}$(f)) dB in the frequency range of 80MHz to 600MHz.

When doing the test, DUT should be set to Slave Mode of operation and not transmit any test symbols.

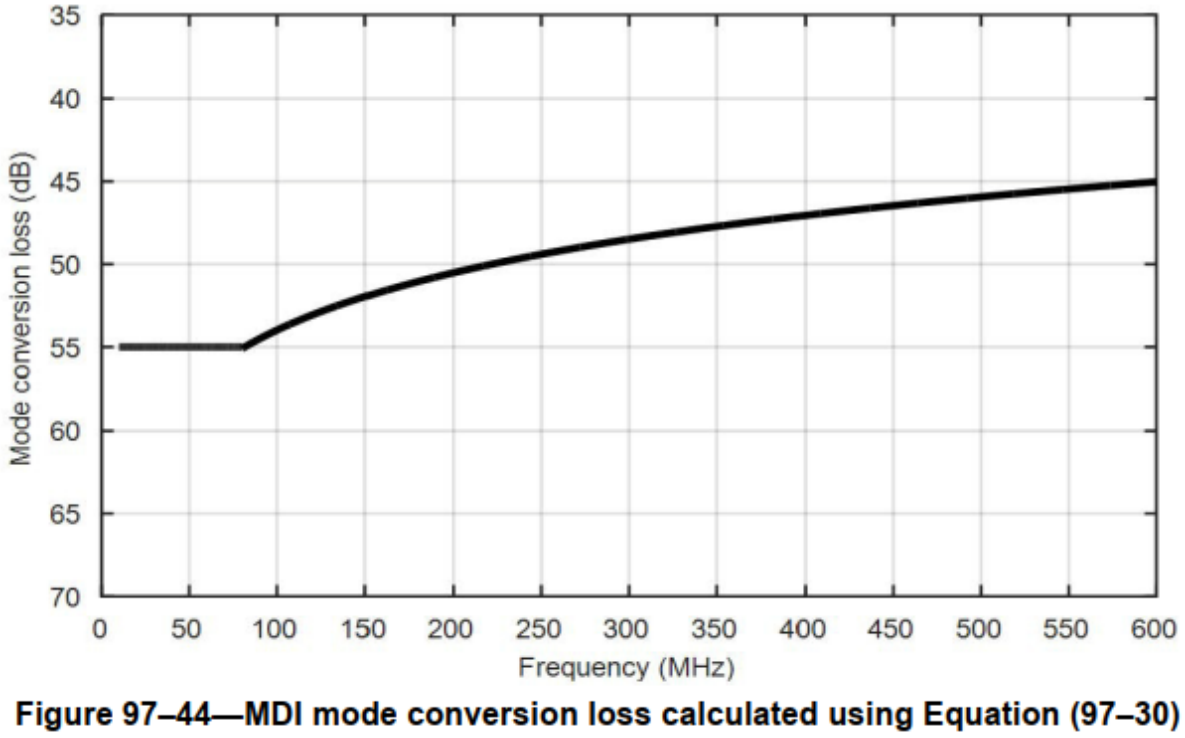


Figure 6-20 Limit for MDI Mode Conversion Loss

6.5.4 Test Result Reference

The test result of the MDI mode conversion loss is shown in Figure 6-21. The waveform details are shown in Figure 6-22.

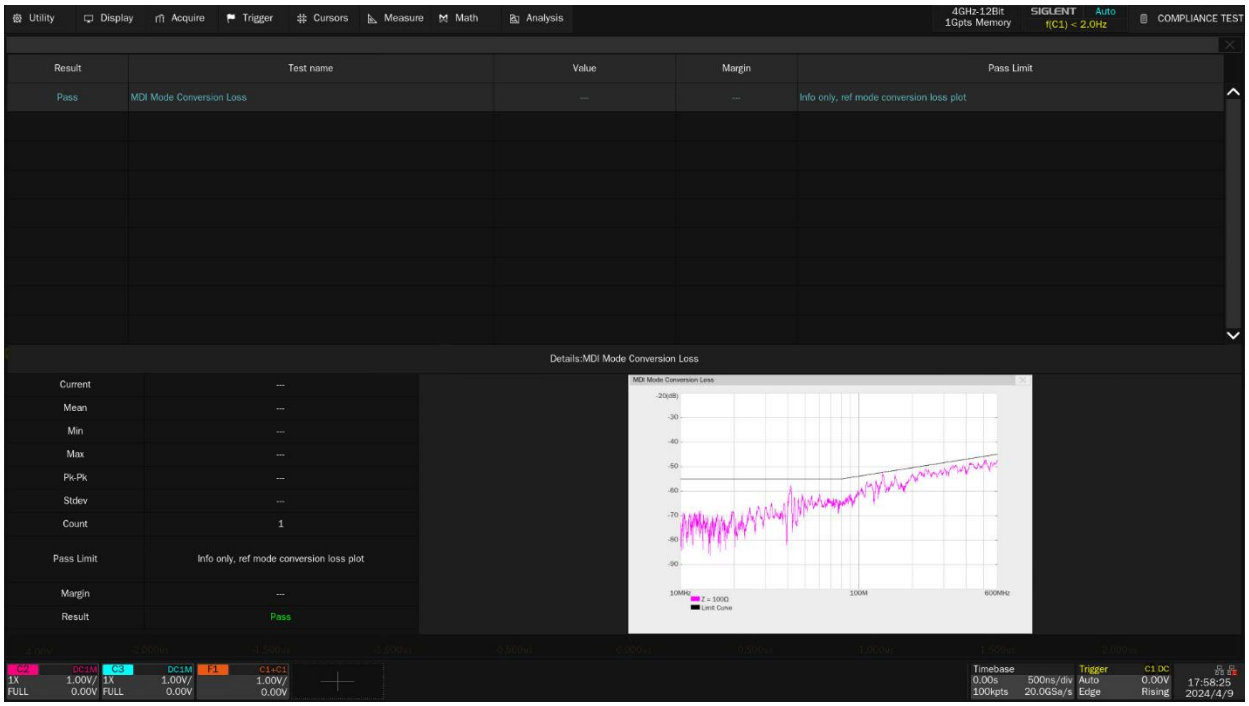


Figure 6-21 Test result of the MDI mode conversion loss

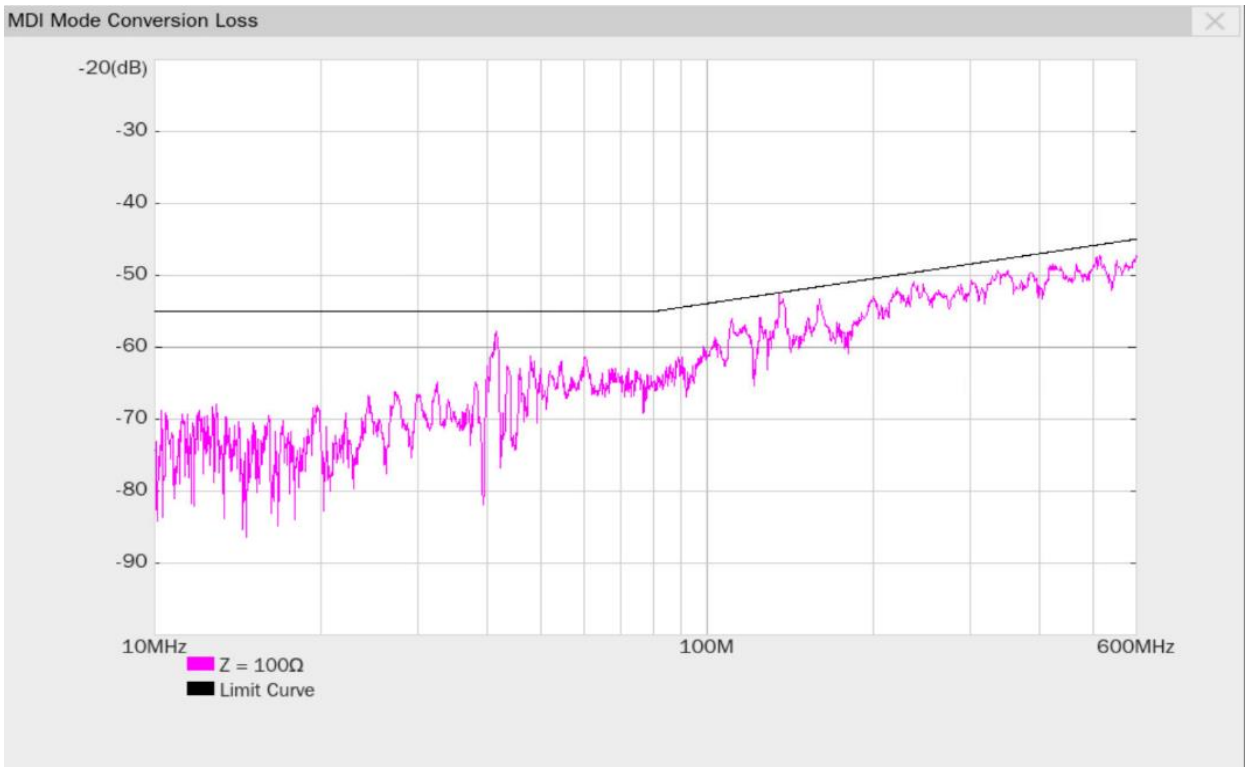


Figure 6-22 Waveform details of the MDI mode conversion loss

6.6 Transmitter Power Spectral Density (PSD) and Peak Differential Output Tests

Section 97.5.3.4 of IEEE Std 802.3bp standard specifies that when DUT is set in Test Mode 5, the transmit power shall be less than 5 dBm. The Transmitter Power Spectral Density and Peak

Differential Output shall be within the specified range according to the specification.

6.6.1 Test Environment and Connectivity

6.6.1.1 Use the Oscilloscope to do PSD and Peak Differential Output Tests

Test environment and connection by using an Oscilloscope for power spectral density and peak differential output tests are the same as <6.2.1 Test Environment and Connectivity> chapter.
The test environment and connection by using a pair of SMA cables is shown in Figure 6-5.
The test environment and connection by using an active differential probe is shown in Figure 6-6.

6.6.1.2 Use a Spectrum Analyzer to do PSD Test

A Spectrum Analyzer can be used to measure the transmitter power spectral density (PSD) to achieve higher measurement accuracy comparing to the Oscilloscope. The connection diagram is shown in Figure 6-23.The measurement procedure is as follows:

(1) Configure the DUT to output the Test Mode 5 signal.

(2) Solder the cable of DUT to TP3 on section ③ of the test fixture.

(3) Use a SMA cable to connect the J12 connector on section ③ of the test fixture to the RF INPUT port on the Spectrum Analyzer.

(4) Use a USB cable to connect the USB Host port on the Oscilloscope to the USB Device port on the Spectrum Analyzer.

(5) In the user interface's **Test Select** tab of the Oscilloscope, click **Transmitter Power Spectral Density**. In the **Configure** tab, click **Transmitter Power Spectral Density** -> **Spectrum Analyzer** -> **Connect Test**, the Oscilloscope will detect the Spectrum Analyzer connection status, if the Spectrum Analyzer is detected, then the Model Name of Spectrum Analyzer will appear, and the Oscilloscope will automatically carry out the Spectrum Analyzer setting (automatically setting only supports Siglent's model). The following is a list of Spectrum Analyzer setup:
   - Measurement Unit: dBm;
   - Start Frequency: 0.3MHz (Note: in the specification, the start frequency is 0Hz, but the test result is affected by the LO frequency of the Spectrum Analyzer, so the start frequency is 0.3MHz in this test run);
   - Stop Frequency: 200MHz;
   - RBW: 100kHz;
   - VBW: 300kHz;
   - Detector: RMS Average;
   - Frequency Sweep time: 60s.

(6) On the Oscilloscope Click **Run Test**, and click **Run Test** when the pop-up window appears.

The Oscilloscope will automatically acquire the power spectral density data tested by the Spectrum Analyzer and plots the curve, then Oscilloscope outputs the test result.

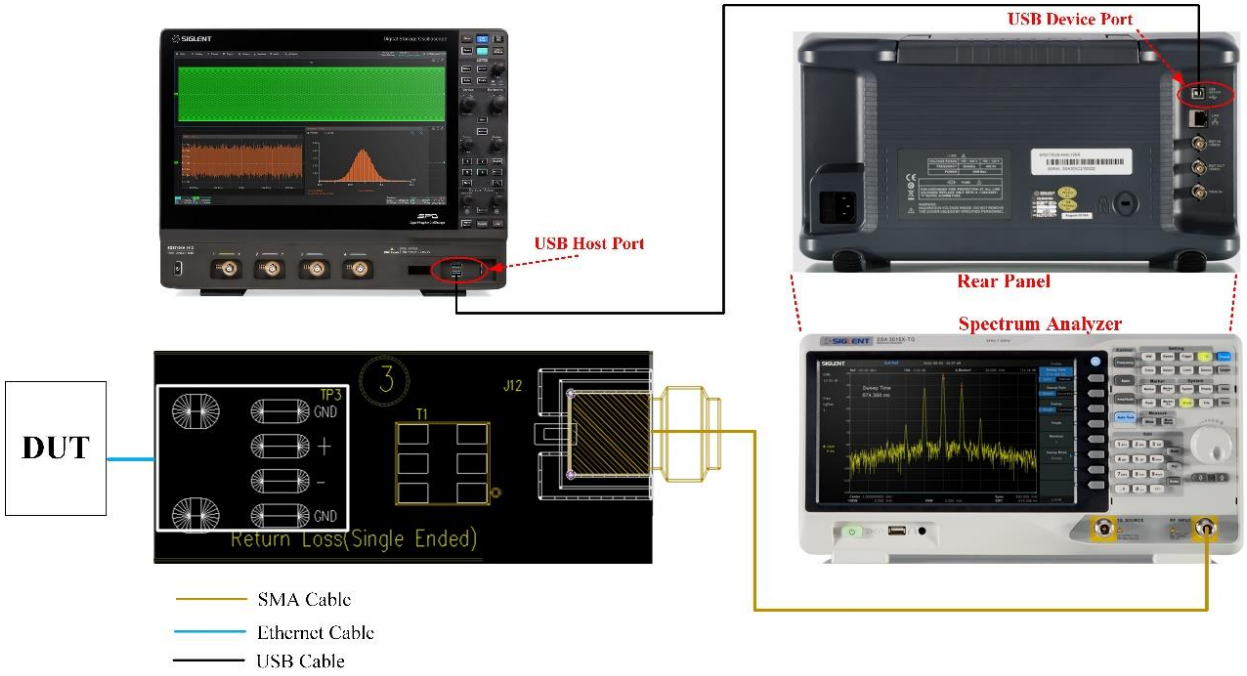


Figure 6-23 Test environment and connection for PSD test by using a Spectrum Analyzer

6.6.2 Test Procedure

(1) Configure the DUT to output test mode 5 signal.

(2) Select the **Transmitter Power Spectral Density and Peak Differential Output** In the **Test Select** tab.

(3) Set the probe type (differential probe or single-ended input), source channel, average number, and whether to use Spectrum Analyzers to do the PSD test in the **Configure** tab.

(4) Check the correctness of the test environment setup in the **Connect** tab.

(5) Click **Run Test** .

(6) If the system is not physically configured to perform this test, the application will return to the **Connect** step to prompt you to change the physical configuration. When you have completed these instructions, click **Run Test** button to resume the test run.

(7) During the test, the Oscilloscope will automatically verify whether the correct test signal is present on the configured DUT “Source” channel, if effective signal is detected, the Oscilloscope will configure the correct trigger level to capture the signal. After finishing the tests, the Oscilloscope will output the test results.

If you choose to use the Spectrum Analyzers to measure the transmitter power spectral density, the Oscilloscope will control the Spectrum analyzers to perform the measurements and plot the curve according to the Spectrum analyzer’s measurement then output the test results.

6.6.3 Algorithm

(1) transmitter Power spectral density (PSD)

Transmitter Power spectral density (PSD) is specified according to the Section 96.5.3.4 of IEEE Std 802.3bp.

In test mode 5, the transmit power shall be less than 5 dBm and the power spectral density of the transmitter, measured into a 100 Ω load using the specified test fixture, shall be between the upper and lower masks specified in Figure 6-24. The measurements need to be calibrated for insertion loss of the differential Balun used in the test if a Spectrum Analyzer is used to do the PSD test. The resolution bandwidth of 100 kHz and sweep time of larger than 1 second are considered in PSD measurement.

$$UpperPSD(f) = \begin{cases} -80 & \text{dBm/Hz} \quad 0 < f \le 100 \\ -76 - \frac{f}{25} & \text{dBm/Hz} \quad 100 < f \le 400 \\ -85.6 - \frac{f}{62.5} & \text{dBm/Hz} \quad 400 < f \le 600 \end{cases} \tag{97–14}$$

$$LowerPSD(f) = \begin{cases} -86 & \text{dBm/Hz} \quad 40 < f \le 100 \\ -82 - \frac{f}{25} & \text{dBm/Hz} \quad 100 < f \le 400 \end{cases} \tag{97–15}$$

where

f is the frequency in MHz

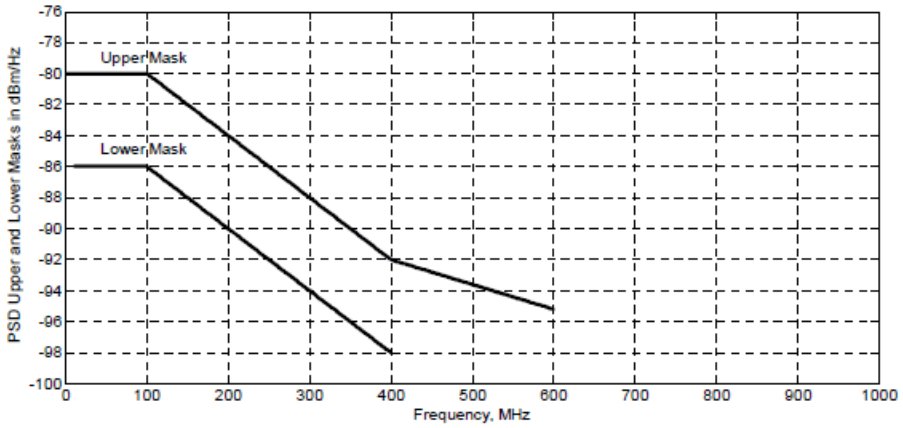


Figure 97–34—Transmitter Power Spectral Density, upper and lower masks

Figure 6-24 Transmitter PSD test, upper and lower masks

(2) Peak differential output

Section 96.5.3.5 of IEEE Std 802.3bp specification specifies that, when DUT is in Test Mode 5 and measured with 100 Ω termination, transmit differential signal at MDI shall be less than 1.30 V peak-to-peak.

6.6.4 Test Results Reference

The test results for the transmitter power spectral density and peak differential output are shown in Figure 6-25, and the waveform details for the transmitter power spectral density is shown in Figure 6-26.

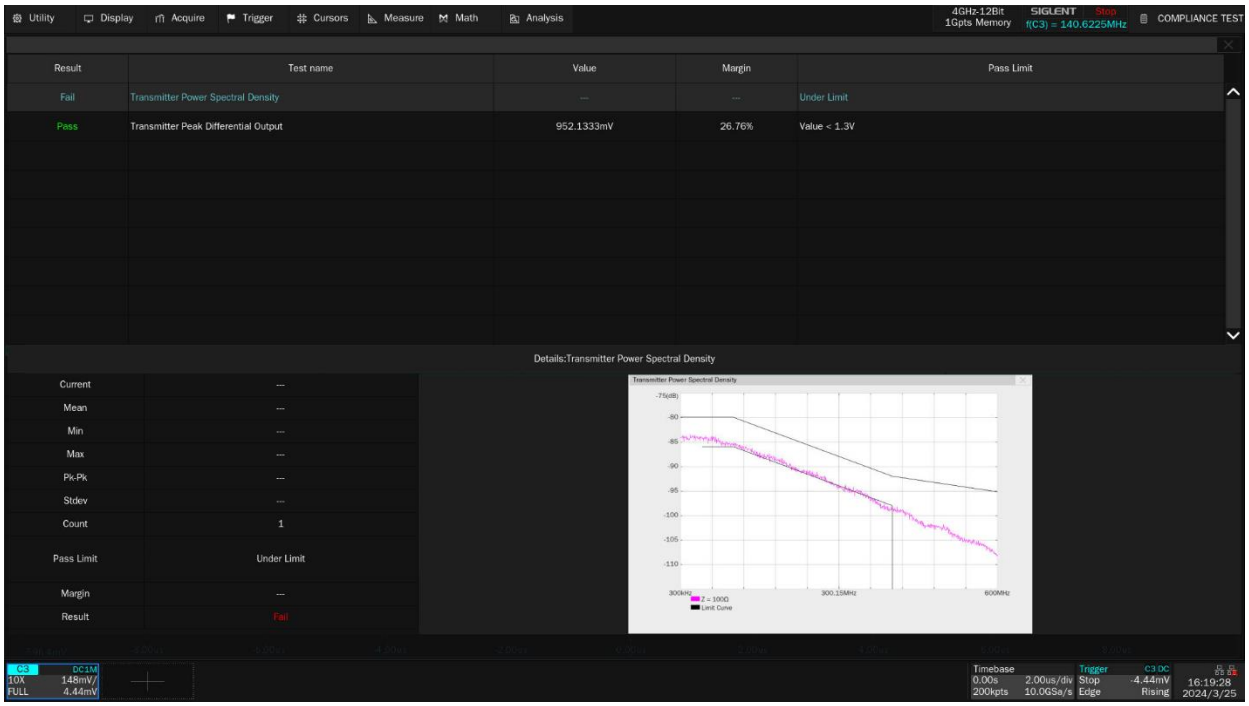


Figure 6-25 PSD and peak differential output test results

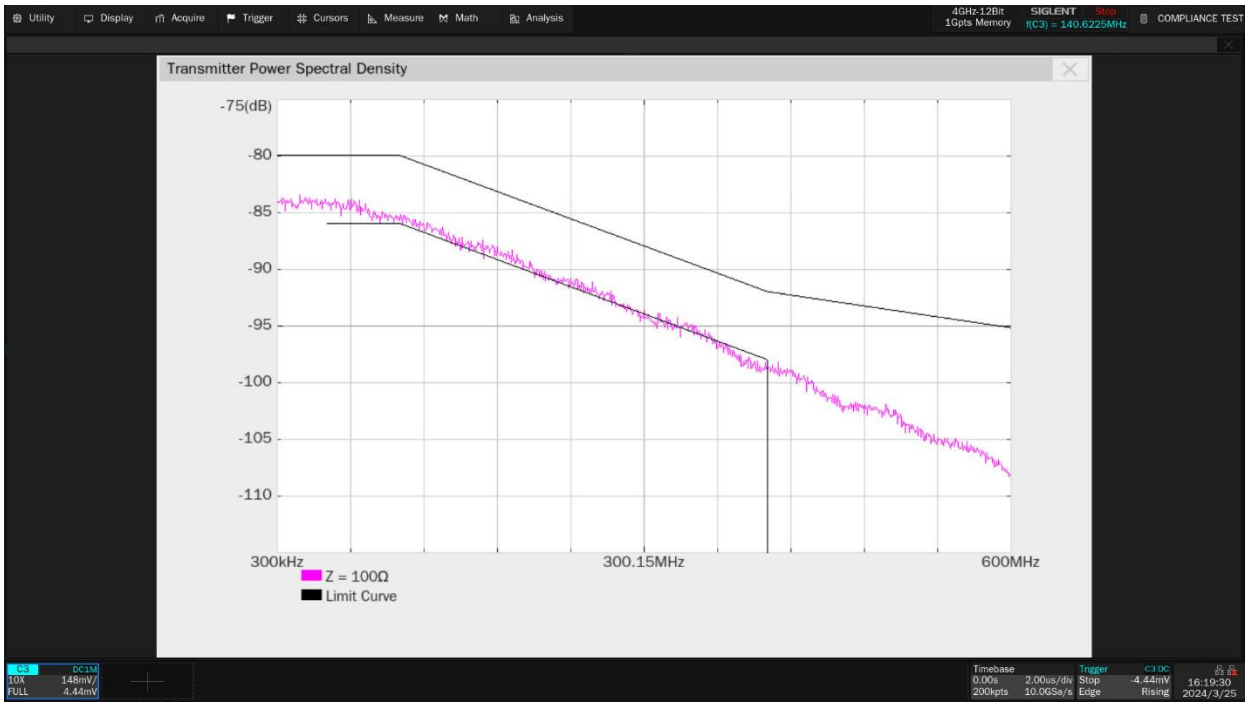


Figure 6-26 Details of transmitted power spectral density waveform

6.7 Transmitter Output Droop Tests

Section 97.5.3.1 of the IEEE Std 802.3bp specification specified that when the DUT enters Test Mode 6, the magnitude of both the positive and negative droop shall be less than 10%, measured with respect to an initial value at 4 ns after the zero crossing and a final value at 16 ns after the zero crossing (12 ns period).

6.7.1 Test Environment and Connectivity

Test environment and connection by using Oscilloscope for transmitter output droop test is the same as <6.2.1 Test Environment and Connectivity> chapter.

The test environment and connection by using a pair of SMA cables is shown in Figure 6-5.

The test environment and connection by using an active differential probe is shown in Figure 6-6.

6.7.2 Test Procedure

(1) Configure the DUT to output test mode 6 signal.

(2) Select the **Transmitter Output Droop** In the **Test Select** tab.

(3) Set the probe type (differential probe or single-ended input), source channel, average number in the **Configure** tab.

(4) Check the correctness of the test environment setup in the **Connect** tab.

(5) Click **Run Test** .

(6) If the system is not physically configured to perform this test, the application will return to the **Connect** step to prompt you to change the physical configuration. When you have completed these instructions, click **Run Test** button to resume the test run.

(7) During the test, the Oscilloscope will automatically verify whether the correct test signal is present on the configured DUT “Source” channel, if effective signal is detected, the Oscilloscope will configure the correct trigger level to capture the signal. After finishing the tests, the Oscilloscope will output the test results.

6.7.3 Algorithm

Section 97.5.3.1 of the IEEE Std 802.3bp specification specified that when the DUT enters Test Mode 6, the magnitude of both the positive and negative droop shall be less than 10%, measured with respect to an initial value at 4 ns after the zero crossing and a final value at 16 ns after the zero crossing (12 ns period), which is shown as Figure 6-27.

The Oscilloscope triggers the Test Mode 6 signal on the rising and falling edge and determines the time the initial voltage value at 4 ns after the zero crossing and a final value at 16 ns after the zero crossing. The droop is calculated as follows:

$$\text{Droop} = 100\ \% \times (Vd/Vpk)$$

Vpk is the initial signal amplitude at 4ns after the zero-crossing.

Vd is the amplitude of the droop.

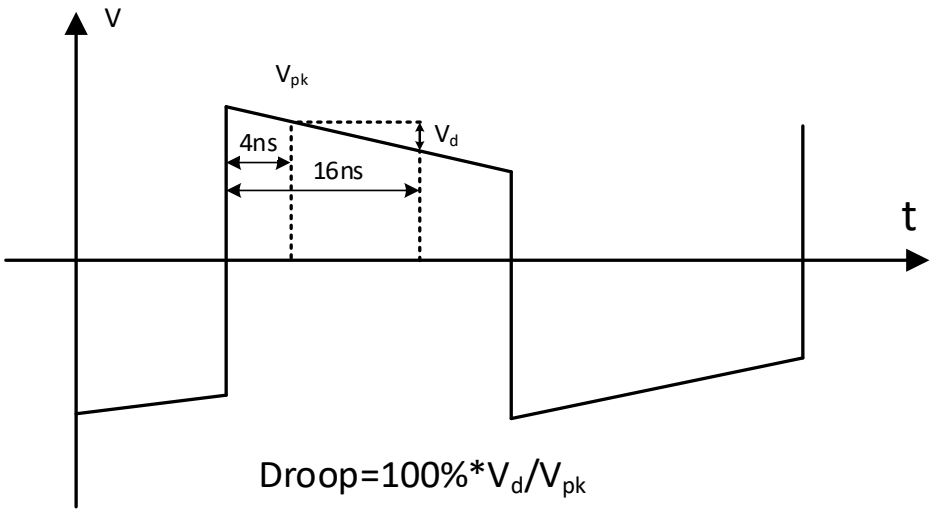


Figure 6-27 The output waveform of Test Mode 6

6.7.4 Test Results Reference

The transmitter output droop test results are shown in Figure 6-28.

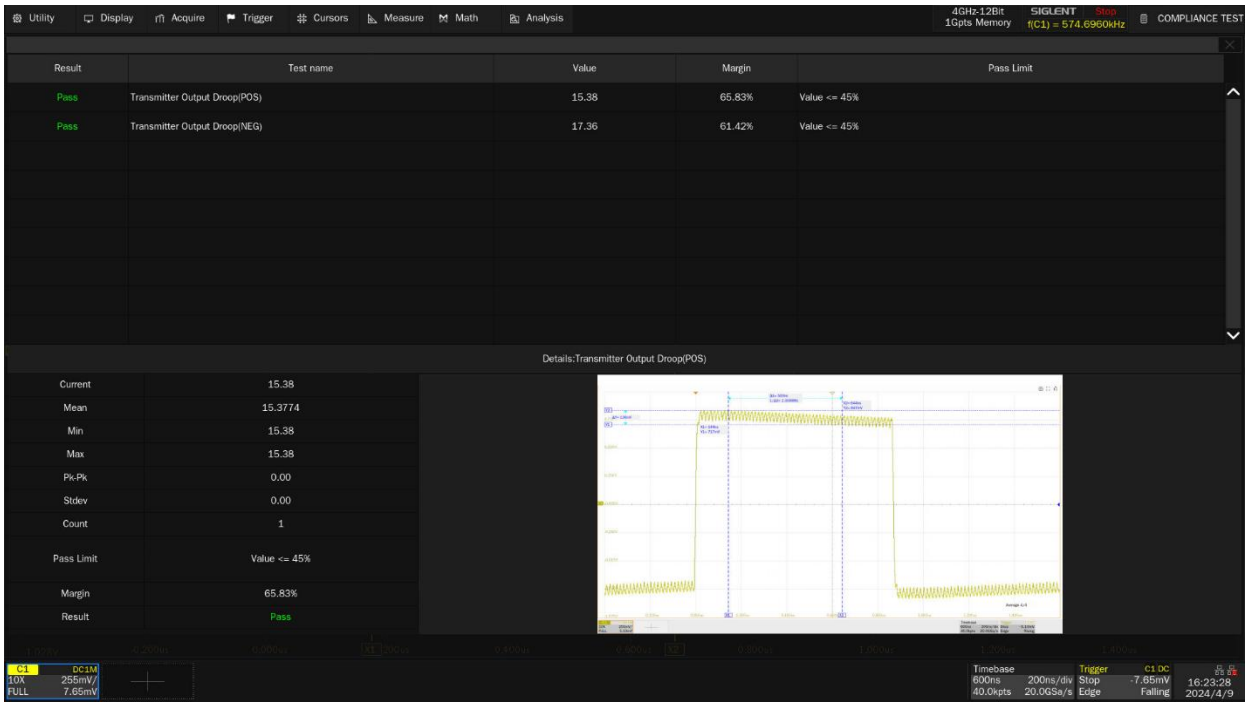


Figure 6-28 Test results of transmitter output droop

The details of the test waveform for transmitter output droop (positive edge) are shown in Figure 6-29.

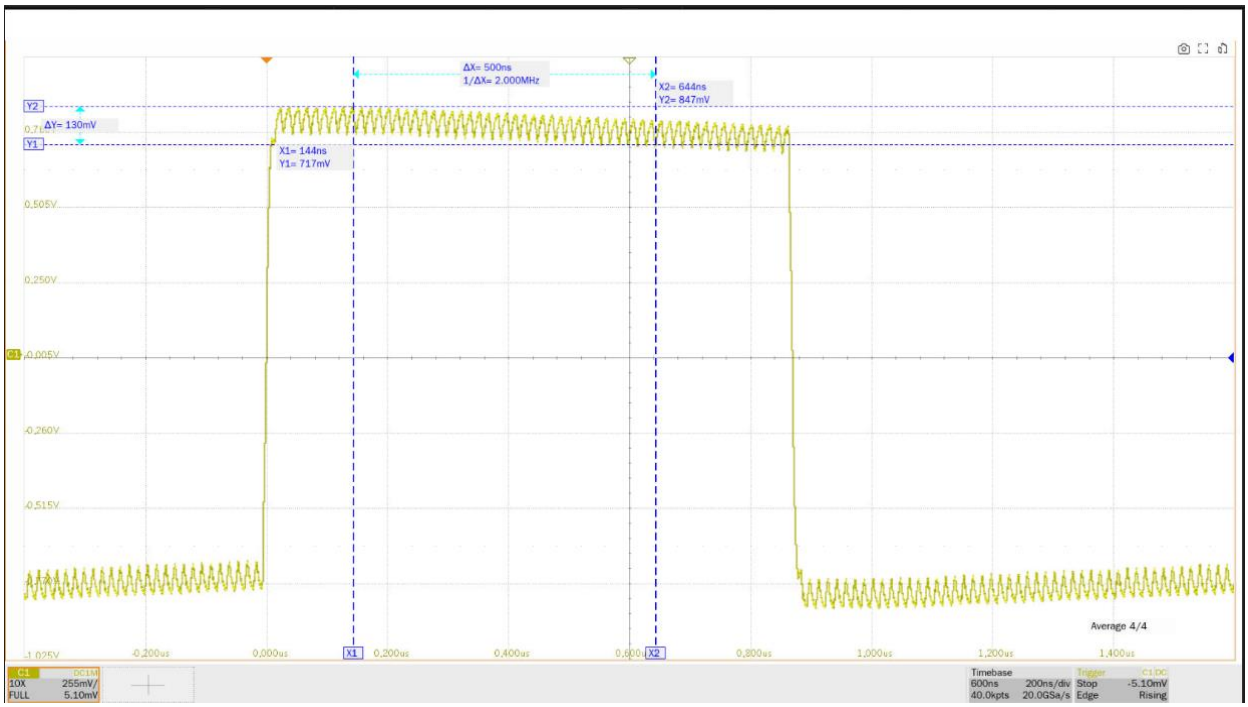


Figure 6-29 Waveform details for positive edge droop test of the transmitter

About SIGLENT

SIGLENT is an international high-tech company, concentrating on R&D, sales, production and services of electronic test & measurement instruments.

SIGLENT first began developing digital oscilloscopes independently in 2002. After more than a decade of continuous development, SIGLENT has extended its product line to include digital oscilloscopes, isolated handheld oscilloscopes, function/arbitrary waveform generators, RF/MW signal generators, spectrum analyzers, vector network analyzers, digital multimeters, DC power supplies, electronic loads and other general purpose test instrumentation. Since its first oscilloscope was launched in 2005, SIGLENT has become the fastest growing manufacturer of digital oscilloscopes. We firmly believe that today SIGLENT is the best value in electronic test & measurement.

Headquarters:

SIGLENT Technologies Co., Ltd
Add: Bldg No.4 & No.5, Antongda Industrial Zone, 3rd Liuxian Road, Bao'an District, Shenzhen, 518101, China
Tel: + 86 755 3688 7876
Fax: + 86 755 3359 1582
Email: sales@siglent.com
Website: int.siglent.com

North America:

SIGLENT Technologies America, Inc
6557 Cochran Rd Solon, Ohio 44139
Tel: 440-398-5800
Toll Free: 877-515-5551
Fax: 440-399-1211
Email: info@siglentna.com
Website: www.siglentna.com

Europe:

SIGLENT Technologies Germany GmbH
Add: Staetzlinger Str. 70
86165 Augsburg, Germany
Tel: +49(0)-821-666 0 111 0
Fax: +49(0)-821-666 0 111 22
Email: info-eu@siglent.com
Website: www.siglenteu.com

Follow us on
Facebook: SiglentTech